



SRI BHARATHI

ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai)
Kaikkurichi, Pudukkottai -622 303

www.sbec.edu.in

NAAC DOCUMENTS



Quality Indicator Frame Work

Criterion – 2

Teaching-Learning and Evaluation

Submitted by

IQAC

Internal Quality Assurance Cell

Sri Bharathi Engineering College for Women



SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai-25)

Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Criteria 2

Teaching-Learning and Evaluation

350

Key Indicator- 2.3. Teaching- Learning Process (40)

2018-2019

**ELECTRONICS AND
COMMUNICATION ENGINEERING**

PARTICIPATIVE LEARNING

Activity	Number of Students Attended	Page No.
Value Added Course (VAC)	100	3
Workshop	19	53
TOTAL STUDENTS ATTENDED	119	-



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Criteria 2

Teaching-Learning and Evaluation

350

Key Indicator- 2.3. Teaching- Learning Process (40)

2018-2019

**ELECTRONICS AND
COMMUNICATION ENGINEERING**

PARTICIPATIVE LEARNING

VALUE ADDED COURSE



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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

DEPARTMENT CIRCULAR

Date:08.06.2018


Value Added Course offered by the Department of ECE will be conducted for all Second, Third and Final year students on “**Digital System Design with Xilinx**” in association with Maria Academy from 18.06.2018 to 22.06.2018. Certificates will be issued to the eligible participants at the end of the course.

S.No	Name of the Course	Resource Person
1	Digital System Design with Xilinx	Er.A.GANESAN, Software Engineer, Maria Academy, No 58, 17, S Usman Road, Near Bus stand, Kannammamet, T. Nagar, Chennai 600059. Tamil Nadu . Mail.Id: mariatrainingacademy@gmail.com

Cc:

- Principal's Office
- IQAC Coordinator
- Class In charges- II ,III & IV Year
- II ,III & IV Year ECE Students
- Notice Board


Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL
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HoD/ECE
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

Value Added Course on “Digital System Design With Xilinx”

SYLLABUS

S.NO	TOPIC COVERED	DURATION (in hours)	DATE
1	Evolution and Basics of ICs and Digital System Design, Evolution of Integrated Circuits ,Digital Logic Family	2	18.06.2018
2	Basics of Logic gates – Boolean Algebra – Digital circuit design using Boolean Algebra and K – Map.	1	18.06.2018
3	ROM, SPLD, CPLD Architecture and Features of FPGA and designing techniques.	3	18.06.2018
4	Architecture of ROM – ROM Programming – Architecture of SPLDs – SPLDs programming	3	19.06.2018
5	Architecture of CPLDs – Basics of FPGAs– Structure of FPGAs	3	19.06.2018
6	Verilog Coding and Simulation of Digital Systems using Xilinx	3	20.06.2018
7	Verilog HDL Basics- Gate level, Data flow and Behaviour Modelling – Simulation of simple digital circuits	3	20.06.2018
8	Implementation of Digital circuits in FPGA processor Spartan 6 FPGA features	3	21.06.2018
9	Education FPGA kit – FPGA pin assignment	3	21.06.2018
10	Implementation of simple digital circuits using FPGA hardware	3	22.06.2018
11	Interfacing Input /Output devices with FPGA	3	22.06.2018
Total Hours			30

VAC Coordinator


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DEPARTMENT OF ELECTRONICS AN COMMUNICATIONENGINEERING

ACADEMIC YEAR ODD SEMESTER (2018-2019)

STUDENT PARTICIPATION LIST FOR VALUE ADDED PROGRAM


Digital System Design With Xilinx

S.NO	REG.NO	NAME	YEAR & BRANCH
1	912617106001	ABIRAMI.S	II&ECE
2	912617106002	ABISHEKA.S	II&ECE
3	912617106003	ATSHAYA.R	II&ECE
4	912617106004	BAVADHARANI.A	II&ECE
5	912617106005	BHUVANESHWARI.B	II&ECE
6	912617106006	DHIVYA.L	II&ECE
7	912617106007	GOWSALYA.D	II&ECE
8	912617106009	INDHUMATHI.S	II&ECE
9	912617106010	KANIMOZHI.D	II&ECE
10	912617106011	KAVYA.C	II&ECE
11	912617106012	KEERTHANA.G	II&ECE
12	912617106013	MAHESHWARI.G	II&ECE
13	912617106014	MANOHARI.M	II&ECE
14	912617106015	MARAGATHALAKSHMI.S	II&ECE
15	912617106017	SAFRIN NISHA.S	II&ECE
16	912617106018	SUBASHINI.M	II&ECE
17	912617106019	SUBASHINI.T	II&ECE
18	912617106020	VINTHIYA.R	II&ECE
19	912616106001	ABINAYA.R	III&ECE
20	912616106002	AGALYA.A	III&ECE
21	912616106003	ATCHAYA.G	III&ECE
22	912616106004	DEEPA.N	III&ECE
23	912616106005	DHARANIYA.A	III&ECE
24	912616106006	JEEVITHA.U	III&ECE
25	912616106007	MAHESWARI.V	III&ECE

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S.NO	REG.NO	NAME	YEAR & BRANCH
26	912616106008	PAZHANIYAMMAL.R	III &ECE
27	912616106009	PRIYANKA.E	III &ECE
28	912616106010	ROJA.A	III &ECE
29	912616106011	SHANMUGAPRIYA.R	III &ECE
30	912616106012	SHIYAMALA.E	III&ECE
31	912616106013	SIVA BHARATHI.P	III&ECE
32	912616106014	SIVARUBINI.S	III&ECE
33	912616106015	THENMOZHI.A	III&ECE
34	912616106016	VINCY.A	III&ECE
35	912616106302	SANKAVI M	III&ECE
36	912615106001	AARTHI .M	IV&ECE
37	912615106002	ABIRAMI .C	IV&ECE
38	912615106004	AKILA .S	IV&ECE
39	912615106005	ARTHI .M	IV&ECE
40	912615106006	BAVADHARANI .M	IV&ECE
41	912615106007	DIVYABHARATHI .S	IV&ECE
42	912615106008	JAGADESWARI .K	IV&ECE
43	912615106009	MEENAKSHI .R	IV&ECE
44	912615106010	MEENAL .T	IV&ECE
45	912615106012	SARGUNAVALLI .C	IV&ECE
46	912615106013	THENMOZHI .K	IV&ECE
47	912615106014	VENNILA .K	IV&ECE
48	912615106301	MANIMEGALAI .S	IV&ECE
49	912615106701	SARADHA .S	IV&ECE
50	912615106702	KAVIYA .S	IV&ECE


VAC Coordinator


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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
ACADEMIC YEAR ODD SEMESTER (2018-2019)

ATTENDANCE SHEET FOR VALUE ADDED COURSE -DIGITAL SYSTEM DESIGN WITH XILINX

S.No	REG. NO	NAME	YEAR/ BRANCH	18.6.2018		19.6.2018		20.6.2018		21.6.2018		22.6.2018		NO. OF SESSIONS ATTENDED	SIGN OF STUDENT
				F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N		
1	912617106001	ABIRAMI.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S. Abirami
2	912617106002	ABISHEKA.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S. Arka
3	912617106003	ATSHAYA.R	II /ECE	a	/	/	/	/	/	/	/	/	/	9	R. Aditya
4	912617106004	BAVADHARANI.A	II /ECE	a	/	/	/	/	/	/	/	/	/	9	B. Barathi
5	912617106005	BHUVANESHWARI.B	II /ECE	/	/	/	/	/	/	/	/	/	/	10	B. Bhuvaneshwari
6	912617106006	DHIVYA.L	II /ECE	/	/	/	/	/	/	/	/	/	/	10	L. Divya
7	912617106007	GOWSALYA.D	II /ECE	/	/	/	/	/	/	/	/	/	/	10	D. Gowsalya
8	912617106009	INDHUMATHI.S	II /ECE	/	/	/	/	a	/	/	/	/	/	9	S. Indhumathi
9	912617106010	KANIMOZHI.D	II /ECE	/	/	/	/	/	/	/	/	/	/	10	D. Kanimozhi
10	912617106011	KAVYA.C	II /ECE	/	/	/	/	/	/	/	/	/	/	10	C. Kavya
11	912617106012	KEERTHANA.G	II /ECE	/	/	/	/	/	/	/	/	/	/	10	G. Keerthana
12	912617106013	MAHESHWARI.G	II /ECE	/	/	/	/	/	/	/	/	/	/	10	G. Maheswari

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13	912617106014	MANOHARI.M	II /ECE	/	/	/	/	/	/	/	/	/	/	10	M. Anuraj
14	912617106015	MARAGATHA LAKSHMI.S	II /ECE	a	a	/	/	/	/	/	/	/	/	8	S. Maragatha
15	912617106017	SAFRIN NISHA.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S. Safran Nisha
16	912617106018	SUBASHINI.M	II /ECE	/	/	/	/	/	/	/	/	/	/	10	M. Subashini
17	912617106019	SUBASHINI.T	II /ECE	/	/	/	/	a	a	/	/	/	/	8	T. Subini
18	912617106020	VINTHIYA.R	II /ECE	/	/	/	/	/	/	/	/	/	/	10	R. Vinthiya
19	912616106001	ABINAYA.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	R. Abinaya
20	912616106002	AGALYA.A	III/ECE	a	a	/	/	/	/	/	/	/	/	8	A. Agalya
21	912616106003	ATCHAYA.G	III/ECE	/	/	/	/	/	/	/	/	/	/	10	G. Atchaya
22	912616106004	DEEPA.N	III/ECE	/	/	/	/	/	/	/	/	/	/	10	N. Deepa
23	912616106005	DHARANIYA.A	III/ECE	/	/	/	/	a	/	/	/	/	/	9	A. Dharam
24	912616106006	JEEVITHA.U	III/ECE	/	/	/	/	/	/	/	/	/	/	10	U. Jeevitha
25	912616106007	MAHESWARI.V	III/ECE	/	/	/	/	a	a	/	/	/	/	8	V. Maheswari
26	912616106008	PAZHANIYAMMAL.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	P. Pammal
27	912616106009	PRIYANKA.E	III/ECE	/	/	/	/	/	/	/	/	/	/	10	P. Priyanka
28	912616106010	ROJA.A	III/ECE	/	/	/	/	/	/	/	/	/	/	10	R. Raja
29	912616106011	SHANMUGAPRIYA.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	S. Shanmugapriya
30	912616106012	SHIYAMALA.E	III/ECE	/	/	/	/	/	/	/	/	/	/	10	S. Shyamala
31	912616106013	SIVA BHARATHI.P	III/ECE	/	/	/	/	/	/	/	/	/	/	10	P. Sivarubini
32	912616106014	SIVARUBINI.S	III/ECE	/	/	/	/	/	/	/	/	/	/	10	S. Sivarubini
33	912616106015	THENMOZHIA	III/ECE	a	a	/	/	/	/	/	/	/	/	8	T. Thenmozhi

34	912616106016	VINCY.A	III/ECE	/	/	/	/	/	/	/	/	/	/	10	Vincy.B.
35	912616106302	SANKAVI M	III/ECE	/	/	/	/	/	/	/	/	/	/	10	M.Santan
36	912615106001	AARTHI .M	IV/ECE	a	/	/	/	/	/	/	/	/	/	9	M. Arthi
37	912615106002	ABIRAMI .C	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Abirami.c
38	912615106004	AKILA .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Akila.S
39	912615106005	ARTHI .M	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Arthi.M
40	912615106006	BAVADHARANI .M	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Bavadarani
41	912615106007	DIVYABHARATHI .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	DivyaBharathi
42	912615106008	JAGADESWARI .K	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Jagadeswari
43	912615106009	MEENAKSHI .R	IV/ECE	/	/	/	/	/	/	a	a	/	/	8	Meenakshi
44	912615106010	MEENAL .T	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	T. Meenal
45	912615106012	SARGUNAVALLI .C	IV/ECE	a	a	/	/	/	/	/	/	/	/	8	C. Sargunavalli
46	912615106013	THENMOZHI .K	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	K. Thenmozhi
47	912615106014	VENNILA .K	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Vennila.
48	912615106301	MANIMEGALAI .S	IV/ECE	/	/	/	/	/	/	a	/	/	/	9	Manimegalai
49	912615106701	SARADHA .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Saradha.S
50	912615106702	KAVIYA .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Kaviya.S

VAC Coordinator

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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Report on Value Added Course

Title: Digital System Design with Xilinx

Resource Person: **Mr.A.GANESAN**
Software Engineer,
Maria Academy ,
T. Nagar, Chennai 600059.

Date of conduct from : **18.06.2018** To: **22.06.2018** Duration: **30 Hours**

Organized Department : **Electronics and Communication Engineering**

Participant Year: **2/ 3 /4** Semester: **ODD** No. of Students Registered : **50**

Venue: **Seminar Hall, ,Ground Floor, SBECW**

Outcome of Value Added Course (VAC):At the end of Course ,Students can able to

- Design the system meeting the specifications
- Design the data path and the controller(s) to implement the functionality.
- Develop Verilog based programs and simulate digital circuits.
- Analyze a VHDL code and infer what circuit a synthesis tool might generate out of a code.
- Implement digital circuits in Xilinx FPGA processor using Hardware description Language experimentally.
- Design and code to exploit the architectural features of FPGA.

No. of students successfully completed the VAC course is **50 Students** based on the following Assessment process.

Assessment Process

- Students securing **more than 60% on total score** and secured more than **75%** in attendance is eligible to receive the certificate for the VAC course conducted
- Total Score = (0.5 *Attendance in VAC out of 100 percentage + 0.5 *Test mark in VAC out of 100 marks)

VAC Coordinator

HOD/ ECE

Principal

HOD / ECE

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MARIA ACADEMY



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. ATCHAYA.G, III YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.


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Ganesan
RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU .
MAIL. ID: MARIATRainingAcademy@gmail.com

MARIA ACADEMY



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. ABIRAMI.S, II YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

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Ganesan
RESOURCE PERSON

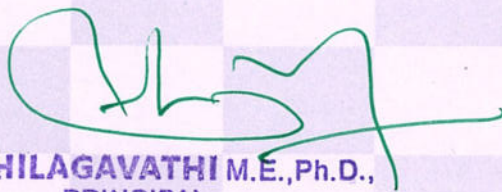
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MAIL. ID: MARIATRainingAcademy@gmail.com

MARIA ACADEMY



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. VENNILA .K, IV YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.



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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Name of the Student :

Year/Sem:

AU Register Number:

Value Added Course on “Digital System Design with Xilinx”

MCQ QUESTIONS (25X1 = 25 Marks)

- Which of the following options comes under the non – saturated logic family in Digital Electronics?
 - Emitter – coupled Logic
 - High-Threshold Logic
 - Integrated – injection Logic
 - Diode – Transistor Logic
- Which characteristic of IC in Digital Circuits represents a function of the switching time of a particular transistor?
 - Fan – out
 - Fan – in
 - Power dissipation
 - Propagation delay
- Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?
 - Two 2 input AND gates
 - Two 3 input AND gates
 - Two 2 input OR gates
 - Two 3 input OR gates
- What must be used along with synchronous control inputs to trigger a change in the flip flop?
 - 0
 - 1
 - Clock
 - Previous output
- What are the basic gates in MOS logic family?
 - NAND and NOR
 - AND and OR
 - NAND and OR
 - AND and NOR
- Which of the following is only predefined physical literal in VHDL?
 - Voltage
 - Time
 - Current
 - Distance
- Access types are similar to _____ in traditional programming languages.
 - Pointers
 - Arrays
 - Structures
 - Files
- Which of the following is default delay in VHDL?
 - Inertial delay
 - Transport delay
 - Delta delay
 - Wire delay
- Transport delay is a kind of _____
 - Synthesis delay
 - Simulation delay
 - Inertial delay
 - Wire delay



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10. A buffer with single input A and single output B has a delay of 20 nanosecond. If the value of input A changes after 10 ns from 0 to 1 and it changes again from 1 to 0 at 20 ns. At what time, the value of output B will be 1, if the transport delay model is used?
- a) 20 ns
b) 30 ns
c) 40 ns
d) Output will remain zero
11. The process used for implementation of sequential logic in VHDL is called _____ process.
- a) Sequential process
b) Combinational process
c) Clocked process
d) Unlocked process
12. A user doesn't want to use the IF statement for detecting clock edge. It is possible to do the same by using any other keyword in VHDL.
- a) True
b) False
13. PLA contains _____
- a) AND and OR arrays
b) NAND and OR arrays
c) NOT and AND arrays
d) NOR and OR arrays
14. A PLA is similar to a ROM in concept except that _____
- a) It hasn't capability to read only
b) It hasn't capability to read or write operation
c) It doesn't provide full decoding to the variables
d) It hasn't capability to write only
15. The complex programmable logic device contains several PLD blocks and _____
- a) A language compiler
b) AND/OR arrays
c) Global interconnection matrix
d) Field-programmable switches
16. Which type of device FPGA are?
- a) SLD
b) SRROM
c) EPROM
d) PLD
17. In FPGA, vertical and horizontal directions are separated by _____
- a) A line
b) A channel
c) A strobe
d) A flip-flop
18. In a digital clock application, the basic frequency must be divided down as _____
- a) 1 Hz
b) 60 Hz
c) 100 Hz
d) 1000 Hz
19. Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?
- a) Simulation
b) Optimization
c) Synthesis
d) Verification


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20. An Antifuse programming technology is predominantly associated with _____.
a) SPLDs
b) FPGAs
c) CPLDs
d) All of the above
21. In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?
a) Floor planning
b) Placement & Routing
c) Testing
d) Extraction
22. In logic synthesis, _____ is an EDIF that gives the description of logic cells & their inter connections.
a) Netlist
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c) Checklist
d) Dualist
23. Which among the following operation/s is/are executed in physical design or layout synthesis stage?
a) Placement of logic functions in optimized circuit in target chip
b) Interconnection of components in the chip
c) Both a and b
d) None of the above
24. In synthesis flow, which stage/s is/are responsible for converting an un optimized boolean description to PLA format?
a) Flattening
b) Translation
c) Optimization
d) All of the above
25. In floorplanning, placement and routing are _____ tools.
a) Front end
b) Back end
c) Both a and b
d) None of the above

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

Value Added Course on “Digital System Design with Xilinx”

MCQ ANSWER KEY

1	A	6	B	11	C	16	D	21	D
2	D	7	A	12	A	17	B	22	A
3	A	8	A	13	A	18	A	23	C
4	C	9	D	14	C	19	C	24	A
5	A	10	B	15	C	20	B	25	B

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Name of the Student : C. Kavya

Year/Sem: II / III

AU Register Number: 912617106011

Value Added Course on “Digital System Design with Xilinx”

MCQ QUESTIONS (25X1 = 25 Marks)

1. Which of the following options comes under the non – saturated logic family in Digital Electronics?
 (a) Emitter – coupled Logic
 (b) High-Threshold Logic
 (c) Integrated – injection Logic
 (d) Diode – Transistor Logic
2. Which characteristic of IC in Digital Circuits represents a function of the switching time of a particular transistor?
 (a) Fan – out
 (b) Fan – in
 (c) Power dissipation
 (d) Propagation delay
3. Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?
 (a) Two 2 input AND gates
 (b) Two 3 input AND gates
 (c) Two 2 input OR gates
 (d) Two 3 input OR gates
4. What must be used along with synchronous control inputs to trigger a change in the flip flop?
 (a) 0
 (b) 1
 (c) Clock
 (d) Previous output
5. What are the basic gates in MOS logic family?
 (a) NAND and NOR
 (b) AND and OR
 (c) NAND and OR
 (d) AND and NOR
6. Which of the following is only predefined physical literal in VHDL?
 (a) Voltage
 (b) Time
 (c) Current
 (d) Distance
7. Access types are similar to _____ in traditional programming languages.
 (a) Pointers
 (b) Arrays
 (c) Structures
 (d) Files
8. Which of the following is default delay in VHDL?
 (a) Inertial delay
 (b) Transport delay
 (c) Delta delay
 (d) Wire delay
9. Transport delay is a kind of _____
 (a) Synthesis delay
 (b) Simulation delay
 (c) Inertial delay
 (d) Wire delay

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10. A buffer with single input A and single output B has a delay of 20 nanosecond. If the value of input A changes after 10 ns from 0 to 1 and it changes again from 1 to 0 at 20 ns. At what time, the value of output B will be 1, if the transport delay model is used?
- a) 20 ns
 b) 30 ns
c) 40 ns
d) Output will remain zero
11. The process used for implementation of sequential logic in VHDL is called _____ process.
- a) Sequential process
b) Combinational process
 c) Clocked process
d) Unlocked process
12. A user doesn't want to use the IF statement for detecting clock edge. It is possible to do the same by using any other keyword in VHDL.
- a) True
 b) False
13. PLA contains _____
- a) AND and OR arrays
b) NAND and OR arrays
c) NOT and AND arrays
d) NOR and OR arrays
14. A PLA is similar to a ROM in concept except that _____
- a) It hasn't capability to read only
b) It hasn't capability to read or write operation
 c) It doesn't provide full decoding to the variables
d) It hasn't capability to write only
15. The complex programmable logic device contains several PLD blocks and _____
- a) A language compiler
b) AND/OR arrays
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d) Field-programmable switches
16. Which type of device FPGA are?
- a) SLD
b) SROM
c) EPROM
 d) PLD
17. In FPGA, vertical and horizontal directions are separated by _____
- a) A line
 b) A channel
c) A strobe
d) A flip-flop
18. In a digital clock application, the basic frequency must be divided down as _____
- a) 1 Hz
b) 60 Hz
c) 100 Hz
d) 1000 Hz
19. Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?
- a) Simulation
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Name of the Student : *A. Dharaniya* Year/Sem: *II/V*

AU Register Number: *912616106005*

Value Added Course on “Digital System Design with Xilinx”

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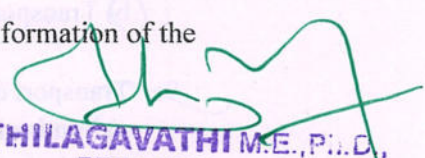
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Name of the Student : T. MEENAL

Year/Sem: IV / VII

AU Register Number: 912615106010

Value Added Course on “Digital System Design with Xilinx”

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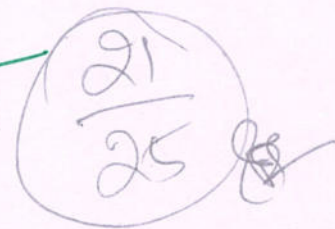
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR ODD SEMESTER (2018-2019)

MARK SHEET FOR VALUE ADDED COURSE- "DIGITAL SYSTEM DESIGN WITH XILINX"

S.NO	REGISTER NUMBER	NAME	YEAR & BRANCH	Attendance (A)		VAC –MCQ TEST (B)		OVERALL MARK(100) (50% of A + 50% of B)
				No.of Sessions Attended	Marks (100)	No.of Correct Answer	Marks (100)	
1	912617106001	ABIRAMI.S	II /ECE	10	100	22	88	94
2	912617106002	ABISHEKA.S	II /ECE	10	100	23	92	96
3	912617106003	ATSHAYA.R	II /ECE	9	90	21	84	87
4	912617106004	BAVADHARANI.A	II /ECE	9	90	20	80	85
5	912617106005	BHUVANESHWARI.B	II /ECE	10	100	19	76	88
6	912617106006	DHIVYA.L	II /ECE	10	100	20	80	90
7	912617106007	GOWSALYA.D	II /ECE	10	100	21	84	92
8	912617106009	INDHUMATHI.S	II /ECE	9	90	19	76	83
9	912617106010	KANIMOZHIL.D	II /ECE	10	100	18	72	86
10	912617106011	KAVYA.C	II /ECE	10	100	22	88	94
11	912617106012	KEERTHANA.G	II /ECE	10	100	20	80	90


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12	912617106013	MAHESHWARI.G	II /ECE	10	100	19	76	88
13	912617106014	MANOHARI.M	II /ECE	10	100	18	72	86
14	912617106015	MARAGATHALAKSHMI.S	II /ECE	8	80	20	80	80
15	912617106017	SAFRIN NISHA.S	II /ECE	10	100	20	80	90
16	912617106018	SUBASHINI.M	II /ECE	10	100	18	72	86
17	912617106019	SUBASHINI.T	II /ECE	8	80	19	76	78
18	912617106020	VINTHIYA.R	II /ECE	10	100	22	88	94
19	912616106001	ABINAYA.R	III /ECE	10	100	19	76	88
20	912616106002	AGALYA.A	III /ECE	8	80	18	72	76
21	912616106003	ATCHAYA.G	III /ECE	10	100	19	76	88
22	912616106004	DEEPA.N	III /ECE	10	100	22	88	94
23	912616106005	DHARANIYA.A	III /ECE	9	90	18	72	81
24	912616106006	JEEVITHA.U	III /ECE	10	100	19	76	88
25	912616106007	MAHESWARI.V	III /ECE	8	80	21	84	82
26	912616106008	PAZHANIYAMMAL.R	III /ECE	10	100	23	92	96
27	912616106009	PRIYANKA.E	III /ECE	10	100	21	84	92
28	912616106010	ROJA.A	III /ECE	10	100	23	92	96
29	912616106011	SHANMUGAPRIYA.R	III /ECE	10	100	19	76	88
30	912616106012	SHIYAMALA.E	III /ECE	10	100	19	76	88
31	912616106013	SIVA BHARATHI.P	III /ECE	10	100	18	72	86
32	912616106014	SIVARUBINI.S	III /ECE	10	100	23	82	91

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33	912616106015	THENMOZHI.A	III /ECE	8	80	18	72	76
34	912616106016	VINCY.A	III /ECE	10	100	18	72	86
35	912616106302	SANKAVI M	III /ECE	10	100	19	76	88
36	912615106001	AARTHI .M	IV/ECE	9	90	18	72	81
37	912615106002	ABIRAMI .C	IV/ECE	10	100	20	80	90
38	912615106004	AKILA .S	IV/ECE	10	100	19	76	88
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41	912615106007	DIVYABHARATHI .S	IV/ECE	10	100	19	76	88
42	912615106008	JAGADESWARI .K	IV/ECE	10	100	17	68	84
43	912615106009	MEENAKSHI .R	IV/ECE	8	80	19	76	78
44	912615106010	MEENAL .T	IV/ECE	10	100	21	84	92
45	912615106012	SARGUNAVALLI .C	IV/ECE	8	80	20	80	80
46	912615106013	THENMOZHI .K	IV/ECE	10	100	15	60	80
47	912615106014	VENNILA .K	IV/ECE	10	100	22	88	94
48	912615106301	MANIMEGALAI .S	IV/ECE	9	90	19	76	83
49	912615106701	SARADHA .S	IV/ECE	10	100	23	92	96
50	912615106702	KAVIYA. S	IV/ECE	10	100	20	80	90

VAC Coordinator


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HoD/ ECE

HOD / ECE
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/EVEN SEMESTER

DEPARTMENT CIRCULAR

Date: 03.12.2018

Value Added Course offered by the Department of ECE will be conducted for all Second, Third and Final year students on “**Antenna Design using High Frequency Simulation Software**” in association with Maria Academy from 10.12.2018 to 14.12.2018. Certificates will be issued to the eligible participants at the end of the course.

S.No	Name of the Course	Resource Person
1	Antenna Design using High Frequency Simulation Software	Er.A.GANESAN, Software Engineer, Maria Academy, No 58, 17, S Usman Road, Near Bus stand, Kannammamet, T. Nagar, Chennai 600 059. Tamil Nadu . Mail.Id: mariatrainingacademy@gmail.com

Cc:

- Principal Office
- IQAC Coordinator
- Class In charges- II ,III & IV Year
- II ,III & IV Year ECE Students
- Notice Board

Rygh
HoD/ECE
HOD / ECE

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KAIKKURICHI,
PUDUKKOTTAI - 622 303.

[Signature]
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Kaikkurichi - 622 303, Pudukkottai Dt.



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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/EVEN SEMESTER

Value Added Course on “Antenna Design Using High Frequency Simulation Software”

SYLLABUS

S.NO	TOPIC COVERED	DURATION (in hours)	DATE
1	Introduction to the course and high-frequency simulation software. Review of antenna fundamentals and electromagnetic theory.	2	10.12.2018
2	Overview of various types of antennas and their applications. Introduction to the chosen simulation software and its interface.	1	10.12.2018
3	Modeling simple wire antennas (dipole, monopole) using the simulation software. Radiation pattern analysis and gain calculations.	3	10.12.2018
4	Design and simulation of patch antennas. Understanding bandwidth, polarization, and impedance matching. Simulation of array antennas (linear and planar arrays).	3	11.12.2018
5	Beamforming techniques and phased arrays.	3	11.12.2018
6	Introduction to microstrip antennas and their design using the software.	3	12.12.2018
7	Design and simulation of helical antennas. Circularly polarized antennas and axial ratio.	3	12.12.2018
8	Optimization algorithms for antenna design.	3	13.12.2018
9	Design and simulation of Yagi-Uda antennas and log-periodic antennas.	3	13.12.2018
10	Antenna arrays with non-uniform excitation.	3	14.12.2018
11	Introduction to antenna measurement techniques and validation of simulation results. Understanding measurement errors and calibration.	3	14.12.2018
Total Hours		30	

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DEPARTMENT OF ELECTRONICS AN COMMUNICATIONENGINEERING
ACADEMIC YEAR EVEN SEMESTER (2018-2019)

STUDENT PARTICIPATION LIST FOR VALUE ADDED PROGRAM

Antenna Design Using High Frequency Simulation Software

S.NO	REG.NO	NAME	YEAR & BRANCH
1	912617106001	ABIRAMI.S	II & ECE
2	912617106002	ABISHEKA.S	II & ECE
3	912617106003	ATSHAYA.R	II & ECE
4	912617106004	BAVADHARANI.A	II & ECE
5	912617106005	BHUVANESHWARI.B	II & ECE
6	912617106006	DHIVYA.L	II & ECE
7	912617106007	GOWSALYA.D	II & ECE
8	912617106009	INDHUMATHI.S	II & ECE
9	912617106010	KANIMOZHI.D	II & ECE
10	912617106011	KAVYA.C	II & ECE
11	912617106012	KEERTHANA.G	II & ECE
12	912617106013	MAHESHWARI.G	II & ECE
13	912617106014	MANOHARI.M	II & ECE
14	912617106015	MARAGATHALAKSHMI.S	II & ECE
15	912617106017	SAFRIN NISHA.S	II & ECE
16	912617106018	SUBASHINI.M	II & ECE
17	912617106019	SUBASHINI.T	II & ECE
18	912617106020	VINTHIYA.R	II & ECE
19	912616106001	ABINAYA.R	III & ECE
20	912616106002	AGALYA.A	III & ECE
21	912616106003	ATCHAYA.G	III & ECE
22	912616106004	DEEPA.N	III & ECE
23	912616106005	DHARANIYA.A	III & ECE
24	912616106006	JEEVITHA.U	III & ECE
25	912616106007	MAHESWARI.V	III & ECE

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S.NO	REG.NO	NAME	YEAR & BRANCH
26	912616106008	PAZHANIYAMMAL.R	III & ECE
27	912616106009	PRIYANKA.E	III & ECE
28	912616106010	ROJA.A	III & ECE
29	912616106011	SHANMUGAPRIYA.R	III & ECE
30	912616106012	SHIYAMALA.E	III & ECE
31	912616106013	SIVA BHARATHI.P	III & ECE
32	912616106014	SIVARUBINI.S	III & ECE
33	912616106015	THENMOZHI.A	III & ECE
34	912616106016	VINCY.A	III & ECE
35	912616106302	SANKAVI M	III & ECE
36	912615106001	AARTHI .M	IV & ECE
37	912615106002	ABIRAMI .C	IV & ECE
38	912615106004	AKILA .S	IV & ECE
39	912615106005	ARTHI .M	IV & ECE
40	912615106006	BAVADHARANI .M	IV & ECE
41	912615106007	DIVYABHARATHI .S	IV & ECE
42	912615106008	JAGADESWARI .K	IV & ECE
43	912615106009	MEENAKSHI .R	IV & ECE
44	912615106010	MEENAL .T	IV & ECE
45	912615106012	SARGUNAVALLI .C	IV & ECE
46	912615106013	THENMOZHI .K	IV & ECE
47	912615106014	VENNILA .K	IV & ECE
48	912615106301	MANIMEGALAI .S	IV & ECE
49	912615106701	SARADHA .S	IV & ECE
50	912615106702	KAVIYA .S	IV & ECE

VAC. Coordinator

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR EVEN SEMESTER (2018-2019)

ATTENDANCE SHEET FOR VALUE ADDED COURSE- ANTENNA DESIGN USING HIGH FREQUENCY SIMULATION SOFTWARE


S.NO	REG. NO	NAME	YEAR/ BRANCH	10.12.2018		11.12.2018		12.12.2018		13.12.2018		14.12.2018		NO. OF SESSIONS ATTENDED	SIGN OF STUDENT
				F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N		
1	912617106001	ABIRAM.I.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S. Abirami
2	912617106002	ABISHEKA.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S. Anika
3	912617106003	ATSHAYA.R	II /ECE	/	/	a	a	/	/	/	/	/	/	8	R. Atal
4	912617106004	BAVADHARANI.A	II /ECE	/	/	/	/	/	/	/	/	/	/	10	A. Bavadhani
5	912617106005	BHUVANESHWARI.B	II /ECE	a	a	/	/	/	/	/	/	/	/	8	B. Bhuvaneshwari
6	912617106006	DHIVYA.L	II /ECE	/	/	/	/	/	/	a	/	/	/	9	L. Divya
7	912617106007	GOWSALYA.D	II /ECE	/	/	/	/	/	/	/	/	/	/	10	D. Gowshalya
8	912617106009	INDHUMATHI.S	II /ECE	a	/	/	/	/	/	/	/	/	/	9	S. Indhumathi
9	912617106010	KANIMOZHI.D	II /ECE	a	/	/	/	/	/	/	/	/	/	9	D. Kanimozhi
10	912617106011	KAVYA.C	II /ECE	/	/	/	/	/	/	/	/	/	/	10	C. Kavya
11	912617106012	KEERTHANA.G	II /ECE	/	/	/	/	/	/	/	/	/	/	10	G. Keerthana

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12	912617106013	MAHESHWARI.G	II /ECE	/	/	/	/	/	/	/	/	/	/	10	G. Maheswari
13	912617106014	MANOHARI.M	II /ECE	/	/	/	/	/	/	/	/	/	/	10	M. Manis
14	912617106015	MARAGATHA LAKSHMIS	II /ECE	/	/	/	/	a	/	/	/	/	/	9	S. Maragathalakshmi
15	912617106017	SAFRIN NISHA.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S. Safrin Nisha
16	912617106018	SUBASHINI.M	II /ECE	/	/	/	/	/	/	/	/	/	/	10	M. Subashini
17	912617106019	SUBASHINI.T	II /ECE	/	/	/	/	/	/	/	/	/	/	10	T. Subini
18	912617106020	VINTHIYA.R	II /ECE	/	/	/	/	/	/	/	/	/	/	10	R. Vinthiya
19	912616106001	ABINAYA.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	R. Abinaya
20	912616106002	AGALYA.A	III/ECE	/	/	/	/	/	/	/	/	/	/	10	A. Agalya
21	912616106003	ATCHAYA.G	III/ECE	/	/	/	/	/	/	/	/	/	/	10	G. Atchaya
22	912616106004	DEEPA.N	III/ECE	/	/	/	/	/	/	/	/	/	/	10	N. Deepa
23	912616106005	DHARANIYA.A	III/ECE	/	/	/	/	/	/	/	/	/	/	10	D. Dhanya
24	912616106006	JEEVITHA.U	III/ECE	/	/	/	/	/	/	/	/	/	/	10	U. Jeevitha
25	912616106007	MAHESWARI.V	III/ECE	/	/	/	/	a	a	/	/	/	/	8	V. Maheswari
26	912616106008	PAZHANIYAMMAL.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	P. Pammal
27	912616106009	PRIYANKA.E	III/ECE	/	/	/	/	/	/	/	/	/	/	10	P. Priyanka E
28	912616106010	ROJA.A	III/ECE	/	/	/	/	/	/	/	/	/	/	10	R. Roja
29	912616106011	SHANMUGAPRIYA.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	S. Shanmugapriya
30	912616106012	SHIYAMALA.E	III/ECE	/	/	/	/	/	/	/	/	/	/	10	S. Shyamala E
31	912616106013	SIVA BHARATHI.P	III/ECE	/	/	/	/	/	/	/	/	/	/	10	P. Sivarathi

32	912616106014	SIVARUBINI.S	III/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Sivz
33	912616106015	THENMOZHIA	III/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Then
34	912616106016	VINCY.A	III/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Vincy A
35	912616106302	SANKAVI M	III/ECE	/	/	/	/	/	/	/	/	/	/	/	10	M. Sankavi
36	912615106001	AARTHI .M	IV/ECE	a	/	/	/	/	/	/	/	/	/	/	9	M. Arathi
37	912615106002	ABIRAMI .C	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Abirami.c
38	912615106004	AKILA .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Akila.S
39	912615106005	ARTHI .M	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Arathi.M
40	912615106006	BAVADHARANI .M	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Bavadarani
41	912615106007	DIVYABHARATHI .S	IV/ECE	/	/	/	/	/	/	a	/	/	/	/	9	S. Divyabharathi
42	912615106008	JAGADESWARI .K	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Jagadevini
43	912615106009	MEENAKSHI .R	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Meenakshi
44	912615106010	MEENAL .T	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	T. Meenal
45	912615106012	SARGUNAVALLI .C	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	C. Sargunavalli
46	912615106013	THENMOZHI .K	IV/ECE	/	/	/	/	a	a	/	/	/	/	/	8	K. Thenmozhi
47	912615106014	VENNILA .K	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Vennila
48	912615106301	MANIMEGALAI .S	IV/ECE	a	/	/	/	/	/	/	/	/	/	/	9	Manimegalai
49	912615106701	SARADHA .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	Saradha
50	912615106702	KAVIYA .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	/	10	S. Kaviya

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VAC Coordinator


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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Report on Value Added Course

Title: Antenna Design using High Frequency Simulation Software

Resource Person: **Mr.A.GANESAN**
Software Engineer,
Maria Academy ,
T. Nagar, Chennai 600059.

Date of conduct from : **10.12.2018** To: **14.12.2018** Duration: **30 Hours**

Organized Department : **Electronics and Communication Engineering**

Participant Year: **2/ 3 /4** Semester: **EVEN** No. of Students Registered : **50**

Venue: **Seminar Hall, ,Ground Floor, SBECW**


Outcome of Value Added Course (VAC) :At the end of Course ,Students can able to

- Design and or develop a prototype in the area of passive/Active circuits/Antennas.
- Design and analyze various antennas.
- Develops an idea to compare the performance of different types of antennas.
- Develops an insight to optimize different performance parameters of antenna to have more advance performance.
- Creates an interest to design a new form of antenna which can be implemented in specific wireless applications.
- Design and analysis of Microwave Antennas Using HFSS.

No. of students successfully completed the VAC course is **50 Students** based on the following Assessment process.

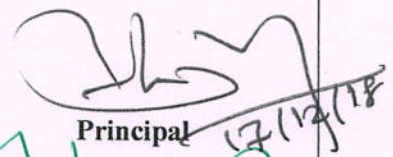
Assessment Process

- Students securing **more than 60% on total score** and secured more than **75%** in attendance is eligible to receive the certificate for the VAC course conducted
- Total Score = (0.5 *Attendance in VAC out of 100 percentage + 0.5 *Test mark in VAC out of 100 marks)


VAC Coordinator


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Principal


Dr. S.THILAGAVATHI M.E.,Ph.D
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SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN
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MARIA ACADEMY



CERTIFICATE OF PARTICIPATION

This certificate recognizes that Ms. BAVADHARANI.A, II YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Antenna Design Using High Frequency Simulation Software Conducted from 10.12.2018 to 14.12.2018 during the academic year 2018-2019.

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Kaikkurchi - 622 303, Pudukkottai Dt.

Ganesan
RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU .
MAIL. ID: MARIATRainingAcademy@gmail.com

MARIA ACADEMY



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. DEEPAN, III YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Antenna Design High Frequency Simulation Software Conducted from 10.12.2018 to 14.12.2018 during the academic year 2018-2019.


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PRINCIPAL
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COLLEGE FOR WOMEN
Kaikkurchi - 622 303, Pudukkottai Dt.

Ganesan
RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU .
MAIL. ID: MARIATRainingAcademy@gmail.com

MARIA ACADEMY



CERTIFICATE OF PARTICIPATION

This certificate recognizes that Ms. MEENAL .T, IV YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Antenna Design Using High Frequency Simulation Software Conducted from 10.12.2018 to 14.12.2018 during the academic year 2018-2019.

Dr. **S.THILAGAVATHI** M.E., Ph.D.,
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COLLEGE FOR WOMEN
Kaikkurchi - 622 303, Pudukkottai Dt.

Ganesan
RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU .
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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Name of the Student :

Year/Sem:

AU Register Number:

Value Added Course on “Antenna Design using HFSS”

MCQ QUESTIONS (20X1 = 20 Marks)

1. EIRP in an isotropic antenna stands for _____.
a) Effective isotropic radiated power
b) Equivalent isotropic radiation power
c) Entropic isotropic radiated power
d) Equivalent isolated radiated power
2. What is the gain factor (in dB) of an isotropic radiator in all directions?
a) 1
b) 0
c) Infinity
d) 0db
3. What is the gain factor of an isotropic radiator in all directions?
a) 1
b) 0
c) Infinity
d) 0db
4. What is the shape of isotropic radiation when observed in 3D?
a) Doughnut shaped
b) Spherical
c) Figure of Eight
d) Circle
5. Isotropic radiation is also known as _____.
a) Omni-directional radiation
b) Bi-directional radiation
c) Tri-directional radiation
d) None of the above
6. The characteristics of an antenna's radiation pattern can be represented in _____ number of ways.
a) 2
b) 3
c) 4
d) 4
7. Transmitting antenna has which of the following parameter as a basic requirement.
a) Side lobes are low
b) Efficiency is high
c) High SNR value
d) High SNR value
8. Which of the following is an equation for ERP of an isotropic antenna?
a) $ERP(dBW) = EIRP(dBW) - 2.15dBi$
b) $ERP(dBW) = EIRP(dBW) - 3.15dBi$
c) $ERP(dBW) = EIRP(dBW) + 2.15dBi$
d) $ERP(dBW) = EIRP(dBW) * 2.15dBi$
9. Radiation patterns can be represented in terms of _____ types.
a) Field patterns
b) Power patterns
c) Both a and b
d) Direction pattern

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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/EVEN SEMESTER

Value Added Course on “Antenna Design Using High Frequency Simulation Software”

MCQ ANSWER KEY

1	A	6	B	11	B	16	A
2	D	7	B	12	A	17	B
3	A	8	A	13	A	18	A
4	A	9	C	14	B	19	C
5	A	10	A	15	A	20	C

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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Name of the Student : R. Atshaya

Year/Sem: II/IV

AU Register Number: 912617106003

Value Added Course on “Antenna Design using HFSS”

MCQ QUESTIONS (20X1 = 20 Marks)

17
20

1. EIRP in an isotropic antenna stands for _____.

- a) Effective isotropic radiated power
 b) Equivalent isotropic radiation power
 c) Entropic isotropic radiated power
 d) Equivalent isolated radiated power

2. What is the gain factor (in dB) of an isotropic radiator in all directions?

- a) 1
 b) 0
 c) Infinity
 d) 0db

3. What is the gain factor of an isotropic radiator in all directions?

- a) 1
 b) 0
 c) Infinity
 d) 0db

4. What is the shape of isotropic radiation when observed in 3D?

- a) Doughnut shaped
 b) Spherical
 c) Figure of Eight
 d) Circle

5. Isotropic radiation is also known as _____.

- a) Omni-directional radiation
 b) Bi-directional radiation
 c) Tri-directional radiation
 d) None of the above

6. The characteristics of an antenna's radiation pattern can be represented in _____ number of ways.

- a) 2
 b) 3
 c) 4
 d) 4

7. Transmitting antenna has which of the following parameter as a basic requirement.

- a) Side lobes are low
 b) Efficiency is high
 c) High SNR value
 d) High SNR value

8. Which of the following is an equation for ERP of an isotropic antenna?

- a) $ERP(dBW) = EIRP(dBW) - 2.15dBi$
 b) $ERP(dBW) = EIRP(dBW) - 3.15dBi$
 c) $ERP(dBW) = EIRP(dBW) + 2.15dBi$
 d) $ERP(dBW) = EIRP(dBW) * 2.15dBi$

9. Radiation patterns can be represented in terms of _____ types.

- a) Field patterns
 b) Power patterns
 c) Both a and b
 d) Direction pattern

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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

10. A 2-D radiation pattern graph contains how many coordinates?

- a) 2 b) 3 c) 5 d) 1

11. Antenna can be polarized in _____ ways.

- a) 3 b) 2 c) 5 d) 1

12. An example of circular polarization is _____.

- a) GPS c) TV signals
b) Radio wave d) Mobile communication signals

13. Which of the following is the frequency of horizontal polarization?

- a) 1 GHz c) 15 GHz
b) 10 GHz d) 20 GHz

14. Magnetic field in EM wave is plotted on _____ axis.

- a) X-axis c) Z-axis
 b) Y-axis d) Either a or b

15. Units of Poynting vector is _____.

- a) W/m² b) W/m c) m/W d) wm

16. If the wavelength is bigger than the length of dipole then it is termed as a type of _____ dipole.

- a) Infinitesimal dipole c) Short dipole
b) Long dipole d) Any of the above

17. What is the range of frequency in a V-shaped antenna that operates?

- a) 33 KHz to 300 GHz c) 30 MHz to 300 GHz
 b) 3 to 30 MHz d) 31 KHz to 300 GHz

18. What is the beam width for a half wave dipole antenna?

- a) 90° c) 50°
b) 180° d) 250°

19. What is the impedance of the folded dipole antenna?

- a) 50Ω c) 300Ω
b) 100Ω d) 20Ω

20. Which of the following antennas produce a vertical radiation pattern?

- a) Dipole antenna c) Marconi antenna
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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Name of the Student : A. ROJA

Year/Sem: III / VI

AU Register Number: 912616106010

Value Added Course on “Antenna Design using HFSS”

MCQ QUESTIONS (20X1 = 20 Marks)

19
20

1. EIRP in an isotropic antenna stands for _____.

- a) Effective isotropic radiated power
 b) Equivalent isotropic radiation power
 c) Entropic isotropic radiated power
 d) Equivalent isolated radiated power

2. What is the gain factor (in dB) of an isotropic radiator in all directions?

- a) 1
 b) 0
 c) Infinity
 d) 0db

3. What is the gain factor of an isotropic radiator in all directions?

- a) 1
 b) 0
 c) Infinity
 d) 0db

4. What is the shape of isotropic radiation when observed in 3D?

- a) Doughnut shaped
 b) Spherical
 c) Figure of Eight
 d) Circle

5. Isotropic radiation is also known as _____.

- a) Omni-directional radiation
 b) Bi-directional radiation
 c) Tri-directional radiation
 d) None of the above

6. The characteristics of an antenna's radiation pattern can be represented in _____ number of ways.

- a) 2
 b) 3
 c) 4
 d) 4

7. Transmitting antenna has which of the following parameter as a basic requirement.

- a) Side lobes are low
 b) Efficiency is high
 c) High SNR value
 d) High SNR value

8. Which of the following is an equation for ERP of an isotropic antenna?

- a) $ERP(dBW) = EIRP(dBW) - 2.15dBi$
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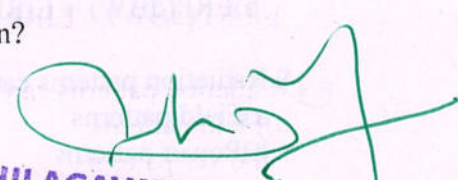
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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Name of the Student : S. SARADHA

Year/Sem: IV | VIII

AU Register Number: 912615706701

Value Added Course on "Antenna Design using HFSS"

MCQ QUESTIONS (20X1 = 20 Marks)

18
20

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR EVEN SEMESTER (2018-2019)

MARK SHEET FOR VALUE ADDED COURSE-ANTENNA DESIGN USING HIGH FREQUENCY

SIMULATION SOFTWARE

S.NO	REGISTER NUMBER	NAME	YEAR & BRANCH	Attendance (A)		VAC –MCQ TEST (B)		OVERALL MARK(100) (50% of A + 50% of B)
				No.of Sessions Attended	Marks (100)	No.of Correct Answer	Marks (100)	
1	912617106001	ABIRAM.I.S	II /ECE	10	100	16	80	90
2	912617106002	ABISHEKA.S	II /ECE	10	100	18	90	95
3	912617106003	ATSHAYA.R	II /ECE	8	80	17	85	83
4	912617106004	BAVADHARANI.A	II /ECE	10	100	14	60	80
5	912617106005	BHUVANESHWARI.B	II /ECE	8	80	13	65	73
6	912617106006	DHIVYA.L	II /ECE	9	90	15	75	83
7	912617106007	GOWSALYA.D	II /ECE	10	100	16	80	90
8	912617106009	INDHUMATHI.S	II /ECE	9	90	15	75	83
9	912617106010	KANIMOZHI.D	II /ECE	9	90	15	75	83
10	912617106011	KAVYA.C	II /ECE	10	100	19	95	98
11	912617106012	KEERTHANA.G	II /ECE	10	100	17	85	93
12	912617106013	MAHESHWARI.G	II /ECE	10	100	14	70	85

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13	912617106014	MANOHARI.M	II /ECE	10	100	14	70	85
14	912617106015	MARAGATHALAKSHMI.S	II /ECE	9	90	13	65	78
15	912617106017	SAFRIN NISHA.S	II /ECE	10	100	16	80	90
16	912617106018	SUBASHINI.M	II /ECE	10	100	13	65	83
17	912617106019	SUBASHINI.T	II /ECE	10	100	14	70	85
18	912617106020	VINTHIYA.R	II /ECE	10	100	19	95	98
19	912616106001	ABINAYA.R	III /ECE	10	100	18	90	95
20	912616106002	AGALYA.A	III /ECE	10	100	16	80	90
21	912616106003	ATCHAYA.G	III /ECE	10	100	14	60	80
22	912616106004	DEEPA.N	III /ECE	10	100	18	90	95
23	912616106005	DHARANIYA.A	III /ECE	10	100	14	70	85
24	912616106006	JEEVITHA.U	III /ECE	10	100	14	70	85
25	912616106007	MAHESWARI.V	III /ECE	8	80	15	75	78
26	912616106008	PAZHANIYAMMAL.R	III /ECE	10	100	18	90	95
27	912616106009	PRIYANKA.E	III /ECE	10	100	16	80	90
28	912616106010	ROJA.A	III /ECE	10	100	19	95	98
29	912616106011	SHANMUGAPRIYA.R	III /ECE	10	100	12	60	80
30	912616106012	SHIYAMALA.E	III /ECE	10	100	14	70	82
31	912616106013	SIVA BHARATHI.P	III /ECE	10	100	13	65	83
32	912616106014	SIVARUBINI.S	III /ECE	10	100	19	95	98
33	912616106015	THENMOZHI.A	III /ECE	10	100	13	65	83
34	912616106016	VINCY.A	III /ECE	10	100	14	70	85


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35	912616106302	SANKAVI M	III /ECE	10	100	14	70	85
36	912615106001	AARTHI .M	IV/ECE	9	90	17	75	83
37	912615106002	ABIRAMI .C	IV/ECE	10	100	18	90	95
38	912615106004	AKILA .S	IV/ECE	10	100	16	80	90
39	912615106005	ARTHI .M	IV/ECE	10	100	15	75	88
40	912615106006	BAVADHARANI .M	IV/ECE	10	100	14	70	85
41	912615106007	DIVYABHARATHI .S	IV/ECE	9	90	16	80	85
42	912615106008	JAGADESWARI .K	IV/ECE	10	100	15	75	88
43	912615106009	MEENAKSHI .R	IV/ECE	10	100	17	85	93
44	912615106010	MEENAL .T	IV/ECE	10	100	15	75	88
45	912615106012	SARGUNAVALLI .C	IV/ECE	10	100	13	65	83
46	912615106013	THENMOZHI .K	IV/ECE	8	80	14	70	75
47	912615106014	VENNILA .K	IV/ECE	10	100	18	90	95
48	912615106301	MANIMEGALAI .S	IV/ECE	9	90	15	75	83
49	912615106701	SARADHA .S	IV/ECE	10	100	18	90	95
50	912615106702	KAVIYA. S	IV/ECE	10	100	14	70	85


VAC Coordinator


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Criteria 2

Teaching-Learning and Evaluation

350

Key Indicator- 2.3. Teaching- Learning Process (40)

2018-2019

**ELECTRONICS AND
COMMUNICATION ENGINEERING
PARTICIPATIVE LEARNING
WORKSHOP**



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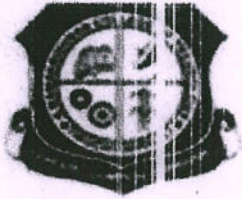
PARTICIPATIVE LEARNING (SYMPOSIUM/WORKSHOP/SEMINAR)

ACADEMIC YEAR 2018-2019

S.No	Register No	Student Name	Year/Sem	Name of the Learning Method
1	912615106001	AARTHI .M	IV/VII	Workshop-Filter design using MATLAB
2	912615106002	ABIRAMI .C		
3	912615106004	AKILA .S		
4	912615106005	ARTHI .M		
5	912615106007	DIVYABHARATHI .S		
6	912615106008	JAGADESWARI .K		
7	912615106010	MEENAL .T		
8	912615106702	KAVIYA .S		
9	912615106013	THENMOZHI .K		
10	912615106014	VENNILA .K		
11	912615106006	BAVADHARANI .M	IV/VII	Workshop-IoT using raspberry Pi
12	912615106701	SARADHA .S		
13	912615106009	MEENAKSHI .R		
14	912615106301	MANIMEGALAI .S		
15	912615106012	SARGUNAVALLI .C		
16	912615106014	VENNILA .K		
17	912616106002	AGALYA.A	III/V	Workshop-IoT using raspberry Pi
18	912616106007	MAHESWARI.V		
19	912616106014	SIVARUBINI.S		


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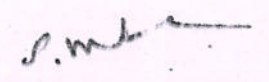
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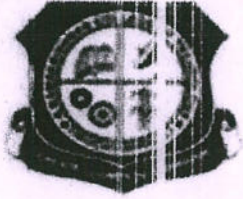
This is to certify that Mr./Ms./Mrs..... M. AARTHI.....
of SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN has participated in one day
workshop on "Filter design and THD analysis for AC-DC converter using
MATLAB" held on 25th July 2018.


Mr. P. Sabarish
Coordinator


Dr. A. Rajkumar
HOD/EEE


Dr. S. THILAGAVATHI M.E., Ph.D.,
PRINCIPAL
SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN,
Kaikkuruchi - 622 303, Pudukkottai Dt.


Dr. S. Muruganandam
Principal



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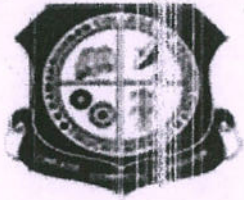
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This is to certify that Mr./Ms./Mrs..... C. ABIRAMI.....
of SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN has participated in one day
workshop on "Filter design and THD analysis for AC-DC converter using
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Mr. P. Sabarish
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Dr. S. Muruganandam
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Dr. S. THILAGAVATHI M.E., Ph.D.,
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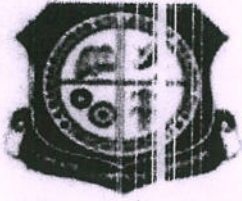
This is to certify that Mr./Ms./Mrs.....*S. AKILA*.....
of *SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN* has participated in one day
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P. Sabarish
Mr. P. Sabarish
Coordinator

A. R. Kumar
Dr. A. R. Kumar
HoD, EEE

S. Thilagavathi
Dr. S. Thilagavathi M.E., Ph.D.
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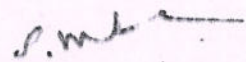
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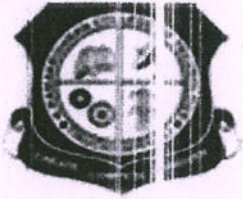
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Mr. P. Sabarish
Coordinator


Dr. A. Rajkumar
HOD/EEE


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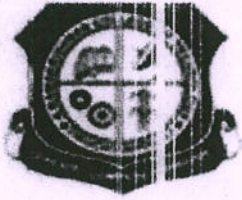
CERTIFICATE

This is to certify that Mr./Ms./Mrs.....*S. DIVYA BHARATHI*.....
of *SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN* has participated in one day
workshop on "Filter design and THD analysis for AC-DC converter using
MATLAB" held on 26th July 2018.

P. Sabarish
Mr. P. Sabarish
Coordinator

A. Rajkumar
Dr. A. Rajkumar
HOD/EEE

S. Muruganandam
Dr. S. Muruganandam
Principal
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PRINCIPAL
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This is to certify that Mr./Ms./Mrs..... *K. JAGADEESWAR!*

of *Sri. BHARATHI..ENGINEERING..COLLEGE FOR..WOMEN*.has participated in one day

workshop on "Filter design and THD analysis for AC-DC converter using

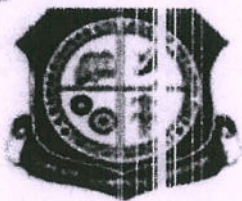
MATLAB" held on 25th July 2018.

P. Sabarish
Mr.P.Sabarish
Coordinator

A. Ajaykumar
Dr. A. Ajaykumar
HOD/EEE

S. Thilagavathi
Dr. S. THILAGAVATHI M.E., Ph.D.,
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S. Muruganandam
Dr.S.Muruganandam
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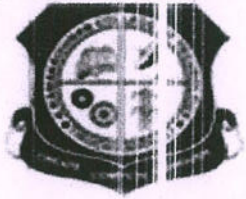
This is to certify that Mr./Ms./Mrs..... T. MEENAL.....
of SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN has participated in one day
workshop on "Filter design and THD analysis for AC-DC converter using
MATLAB" held on 25th July 2018.


Mr. P. Sabarish
Coordinator


Dr. A. Rajkumar
HOD/EEE


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Principal

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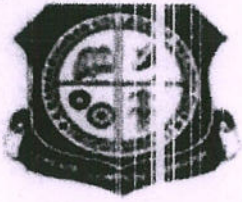
This is to certify that Mr./Ms./Mrs..... S. KAVIYA.....
of SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN has participated in one day
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MATLAB" held on 25th July 2018.


Mr. P. Sabarish
Coordinator


Dr. A. Rajkumar
Hbl/EEE


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Dr. S. Muruganandam
Principal



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of *SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN* has participated in one day
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P. Sabarish
Mr. P. Sabarish
Coordinator

A. Ajay Kumar
Dr. A. Ajay Kumar
HOD VEEE

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Dr. S. Muruganandam
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This is to certify that Mr./Ms./Mrs.....*K. VENNILA*.....
of *SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN* has participated in one day
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Mr.P.Sabarish
Coordinator

A. Rajkumar
Dr. A.Rajkumar
HoD/EEE

S. Muruganandam
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website: www.mzcet.in, Fax: +91 8030723678.



CERTIFICATE

This is to certify that BAVADHARANI. M - IV YEAR / ECE of
SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN has
participated in the one day workshop on IoT using Raspberry Pi organised by the Department of
Computer Science and Engineering in association with the Computer Society of India at
Mount Zion College of Engineering and Technology, on August 29, 2018.

A. V. V. / 29/8/18
COORDINATOR


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This is to certify that SARADHA.S - IV YEAR / ECE of
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A. V. S. S. S. S. S.
COORDINATOR

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CERTIFICATE

This is to certify that MEENAKSHI.R IV YEAR / ECE of
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Computer Science and Engineering in association with the Computer Society of India at
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A. A. 29/8/18
COORDINATOR


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CERTIFICATE

This is to certify that MONIMEGALAI.S YEAR I/ECE of
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Computer Science and Engineering in association with the Computer Society of India at
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A-11/29/8/18
COORDINATOR


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CERTIFICATE

This is to certify that SARGUNAVALLI. C. YEAR / ECE of
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A. H. P. 29/8/18
COORDINATOR


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CERTIFICATE

This is to certify that VENNILA-K YEAR /ECE of
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A. V. S. / 29/8/18
COORDINATOR


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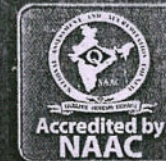
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This is to certify that AGIALYA . A - III YEAR /ECE of
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A. H. 29/8/18

COORDINATOR

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CERTIFICATE

This is to certify that MAHESWARI.V - III YEAR /ECE of
SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN has
participated in the one day workshop on IoT using Raspberry Pi organised by the Department of
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A. V. P. 29/8/18

COORDINATOR

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CERTIFICATE

This is to certify that SIVARUBINI.S - III YEAR /ECE of
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A. H. S. S. S. S.
COORDINATOR

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