SRI BHARATHI

ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai)

Kaikkurichi, Pudukkottai -622 303

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NAAC DOCUMENTS

Quality Indicator Frame Work

Criterion – 1

CURRICULAR ASPECTS

Submitted by

IQAC

Internal Quality Assurance Cell

Sri Bharathi Engineering College for Women

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN
Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)
KAIKKURUCHI, PUDUKOTTAI – 622 303

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019 / ODD SEMESTER

1.2 Academic Flexibility (30)

1.2.1 Number of Certificate/Value added courses offered and online courses of MOOCs, SWAYAM, NPTEL etc. (where the students of the institution have enrolled and successfully completed during the last five years)

AND

1.2.2 Percentage of students enrolled in Certificate/ Value added courses and also completed online courses of MOOCs, SWAYAM, NPTEL etc. as against the total number of students during the last five years

VAC Title:	**DIGITAL SYSTEM DESIGN WITH XILINX**				
Resource Person:	**Er.A.GANESAN,** Software Engineer, Maria Academy,Chennai.				
Date of conduct from :	**18.06.2018**	**To:**	**22.06.2018**	**Duration:**	**30 Hours**
Organized Department :	**ELECTRONICS AND COMMUNICATION ENGINEERING**				
Participant Year:	**2/3/4**	**Semester:**	**ODD**	**No. of Students Registered :**	**50**
Venue:	**Seminar Hall, ,Ground Floor, SBECW**				

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SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)
Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

DEPARTMENT CIRCULAR

Date:08.06.2018

Value Added Course offered by the Department of ECE will be conducted for all Second, Third and Final year students on "**Digital System Design with Xilinx**" in association with Maria Academy from 18.06.2018 to 22.06.2018. Certificates will be issued to the eligible participants at the end of the course.

S.No	Name of the Course	Resource Person
1	Digital System Design with Xilinx	**Er.A.GANESAN,** Software Engineer, Maria Academy, No 58, 17, S Usman Road, Near Bus stand, Kannammapet, T. Nagar, Chennai 600059. Tamil Nadu . **Mail.Id:**mariatrainingacademy@gmail.com

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HOD / ECE
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PUDUKKOTTAI - 622 303.

Cc:

- Principal's Office
- IQAC Coordinator
- Class In charges- II ,III &IV Year
- II ,III & IV Year ECE Students
- Notice Board

Dr. S.THILAGAVATHI M.E., Ph.D.,
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

Value Added Course on "**Digital System Design With Xilinx**"

SYLLABUS

S.NO	TOPIC COVERED	DURATION (in hours)	DATE
1	Evolution and Basics of ICs and Digital System Design, Evolution of Integrated Circuits ,Digital Logic Family	2	18.06.2018
2	Basics of Logic gates – Boolean Algebra – Digital circuit design using Boolean Algebra and K – Map.	1	18.06.2018
3	ROM, SPLD, CPLD Architecture and Features of FPGA and designing techniques.	3	18.06.2018
4	Architecture of ROM – ROM Programming – Architecture of SPLDs – SPLDs programming	3	19.06.2018
5	Architecture of CPLDs – Basics of FPGAs– Structure of FPGAs	3	19.06.2018
6	Verilog Coding and Simulation of Digital Systems using Xilinx	3	20.06.2018
7	Verilog HDL Basics- Gate level, Data flow and Behaviour Modelling – Simulation of simple digital circuits	3	20.06.2018
8	Implementation of Digital circuits in FPGA processor Spartan 6 FPGA features	3	21.06.2018
9	Education FPGA kit – FPGA pin assignment	3	21.06.2018
10	Implementation of simple digital circuits using FPGA hardware	3	22.06.2018
11	Interfacing Input /Output devices with FPGA	3	22.06.2018
Total Hours		**30**	

VAC Coordinator

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DEPARTMENT OF ELECTRONICS AN COMMUNICATIONENGINEERING

ACADEMIC YEAR ODD SEMESTER (2018-2019)

STUDENT PARTICIPATION LIST FOR VALUE ADDED PROGRAM

Digital System Design With Xilinx

S.NO	REG.NO	NAME	YEAR & BRANCH
1	912617106001	ABIRAMI.S	II&ECE
2	912617106002	ABISHEKA.S	II&ECE
3	912617106003	ATSHAYA.R	II&ECE
4	912617106004	BAVADHARANI.A	II&ECE
5	912617106005	BHUVANESHWARI.B	II&ECE
6	912617106006	DHIVYA.L	II&ECE
7	912617106007	GOWSALYA.D	II&ECE
8	912617106009	INDHUMATHI.S	II&ECE
9	912617106010	KANIMOZHI.D	II&ECE
10	912617106011	KAVYA.C	II&ECE
11	912617106012	KEERTHANA.G	II&ECE
12	912617106013	MAHESHWARI.G	II&ECE
13	912617106014	MANOHARI.M	II&ECE
14	912617106015	MARAGATHALAKSHMI.S	II&ECE
15	912617106017	SAFRIN NISHA.S	II&ECE
16	912617106018	SUBASHINI.M	II&ECE
17	912617106019	SUBASHINI.T	II&ECE
18	912617106020	VINTHIYA.R	II&ECE
19	912616106001	ABINAYA.R	III&ECE
20	912616106002	AGALYA.A	III&ECE
21	912616106003	ATCHAYA.G	III&ECE
22	912616106004	DEEPA.N	III&ECE
23	912616106005	DHARANIYA.A	III&ECE
24	912616106006	JEEVITHA.U	III&ECE
25	912616106007	MAHESWARI.V	III&ECE

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S.NO	REG.NO	NAME	YEAR & BRANCH
26	912616106008	PAZHANIYAMMAL.R	III &ECE
27	912616106009	PRIYANKA.E	III &ECE
28	912616106010	ROJA.A	III &ECE
29	912616106011	SHANMUGAPRIYA.R	III &ECE
30	912616106012	SHIYAMALA.E	III&ECE
31	912616106013	SIVA BHARATHI.P	III&ECE
32	912616106014	SIVARUBINI.S	III&ECE
33	912616106015	THENMOZHI.A	III&ECE
34	912616106016	VINCY.A	III&ECE
35	912616106302	SANKAVI M	III&ECE
36	912615106001	AARTHI .M	IV&ECE
37	912615106002	ABIRAMI .C	IV&ECE
38	912615106004	AKILA .S	IV&ECE
39	912615106005	ARTHI .M	IV&ECE
40	912615106006	BAVADHARANI .M	IV&ECE
41	912615106007	DIVYABHARATHI .S	IV&ECE
42	912615106008	JAGADESWARI .K	IV&ECE
43	912615106009	MEENAKSHI .R	IV&ECE
44	912615106010	MEENAL .T	IV&ECE
45	912615106012	SARGUNAVALLI .C	IV&ECE
46	912615106013	THENMOZHI .K	IV&ECE
47	912615106014	VENNILA .K	IV&ECE
48	912615106301	MANIMEGALAI .S	IV&ECE
49	912615106701	SARADHA .S	IV&ECE
50	912615106702	KAVIYA. S	IV&ECE

VAC Coordinator

HoD/ECE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
ACADEMIC YEAR ODD SEMESTER (2018-2019)

ATTENDANCE SHEET FOR VALUE ADDED COURSE -DIGITAL SYSTEM DESIGN WITH XILINX

S.No	REG. NO	NAME	YEAR/ BRANCH	18.6.2018		19.6.2018		20.6.2018		21.6.2018		22.6.2018		NO. OF SESSIONS ATTENDED	SIGN OF STUDENT
				F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N		
1	912617106001	ABIRAMI.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S.Abirami
2	912617106002	ABISHEKA.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S.Abisheka
3	912617106003	ATSHAYA.R	II /ECE	a	/	/	/	/	/	/	/	/	/	9	R.Atchaya
4	912617106004	BAVADHARANI.A	II /ECE	a	/	/	/	/	/	/	/	/	/	9	A.Bavadharani
5	912617106005	BHUVANESHWARI.B	II /ECE	/	/	/	/	/	/	/	/	/	/	10	B.Bhuvaneshwari
6	912617106006	DHIVYA.L	II /ECE	/	/	/	/	/	/	/	/	/	/	10	L.Dhivya
7	912617106007	GOWSALYA.D	II /ECE	/	/	/	/	/	/	/	/	/	/	10	D.Gowsalya
8	912617106009	INDHUMATHI.S	II /ECE	/	/	/	/	a	/	/	/	/	/	9	S.Indhumathi
9	912617106010	KANIMOZHI.D	II /ECE	/	/	/	/	/	/	/	/	/	/	10	D.Kanimozhi
10	912617106011	KAVYA.C	II /ECE	/	/	/	/	/	/	/	/	/	/	10	C.Kavya
11	912617106012	KEERTHANA.G	II /ECE	/	/	/	/	/	/	/	/	/	/	10	G.Keerthana
12	912617106013	MAHESHWARI.G	II /ECE	/	/	/	/	/	/	/	/	/	/	10	G.Maheswari

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13	912617106014	MANOHARI.M	II /ECE	/	/	/	/	/	/	/	/	/	/	10	M. Manohari
14	912617106015	MARAGATHA LAKSHMI.S	II /ECE	a	a	/	/	/	/	/	/	/	/	8	S. Maragathalak
15	912617106017	SAFRIN NISHA.S	II /ECE	/	/	/	/	/	/	/	/	/	/	10	S. Safrin Nisha
16	912617106018	SUBASHINI.M	II /ECE	/	/	/	/	/	/	/	/	/	/	10	M. Subashini
17	912617106019	SUBASHINI.T	II /ECE	/	/	/	/	a	a	/	/	/	/	8	T. Subashini
18	912617106020	VINTHIYA.R	II /ECE	/	/	/	/	/	/	/	/	/	/	10	R. Vinthiya
19	912616106001	ABINAYA.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	R. Abinaya
20	912616106002	AGALYA.A	III/ECE	a	a	/	/	/	/	/	/	/	/	8	A. Agalya
21	912616106003	ATCHAYA.G	III/ECE	/	/	/	/	/	/	/	/	/	/	10	G. Atchaya
22	912616106004	DEEPA.N	III/ECE	/	/	/	/	/	/	/	/	/	/	10	N. Deepa
23	912616106005	DHARANIYA.A	III/ECE	/	/	/	/	a	/	/	/	/	/	9	A. Dharaniya
24	912616106006	JEEVITHA.U	III/ECE	/	/	/	/	/	/	/	/	/	/	10	U. Jeevitha
25	912616106007	MAHESWARI.V	III/ECE	/	/	/	/	a	a	/	/	/	/	8	V. Maheswari
26	912616106008	PAZHANIYAMMAL.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	Pazhani
27	912616106009	PRIYANKA.E	III/ECE	/	/	/	/	/	/	/	/	/	/	10	Priyanka
28	912616106010	ROJA.A	III/ECE	/	/	/	/	/	/	/	/	/	/	10	Roja
29	912616106011	SHANMUGAPRIYA.R	III/ECE	/	/	/	/	/	/	/	/	/	/	10	Shanpriya
30	912616106012	SHIYAMALA.E	III/ECE	/	/	/	/	/	/	/	/	/	/	10	E. Shiyamala
31	912616106013	SIVA BHARATHI.P	III/ECE	/	/	/	/	/	/	/	/	/	/	10	P. Sivabharathi
32	912616106014	SIVARUBINI.S	III/ECE	/	/	/	/	/	/	/	/	/	/	10	Sivarubini
33	912616106015	THENMOZHI.A	III/ECE	a	a	/	/	/	/	/	/	/	/	8	Thenmozhi

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34	912616106016	VINCY.A	III/ECE	/	/	/	/	/	/	/	/	/	/	10	Vincy.A.
35	912616106302	SANKAVI M	III/ECE	/	/	/	/	/	/	/	/	/	/	10	M. Sankavi
36	912615106001	AARTHI .M	IV/ECE	a	/	/	/	/	/	/	/	/	/	9	M. Aarthi
37	912615106002	ABIRAMI .C	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Abirami.C
38	912615106004	AKILA .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Akila.S
39	912615106005	ARTHI .M	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Arthi.M
40	912615106006	BAVADHARANI .M	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Bavadharani
41	912615106007	DIVYABHARATHI .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	S. Divyabharathi
42	912615106008	JAGADESWARI .K	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Jagadeshwari
43	912615106009	MEENAKSHI .R	IV/ECE	/	/	/	/	/	/	a	a	/	/	8	Meenakshi
44	912615106010	MEENAL .T	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	T. Meenal
45	912615106012	SARGUNAVALLI .C	IV/ECE	a	a	/	/	/	/	/	/	/	/	8	C. Sarguna
46	912615106013	THENMOZHI .K	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	K. Thenmozhi
47	912615106014	VENNILA .K	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Vennila.
48	912615106301	MANIMEGALAI .S	IV/ECE	/	/	/	/	/	/	a	/	/	/	9	
49	912615106701	SARADHA .S	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	Saradha.S
50	912615106702	KAVIYA. S	IV/ECE	/	/	/	/	/	/	/	/	/	/	10	S. Kaviya

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VAC Coordinator

HoD/ ECE

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Report on Value Added Course

Title:	Digital System Design with Xilinx
Resource Person:	**Mr.A.GANESAN** Software Engineer, Maria Academy , T. Nagar, Chennai 600059.

Date of conduct from :	**18.06.2018**	To:	**22.06.2018**	Duration:	**30 Hours**
Organized Department :	**Electronics and Communication Engineering**				
Participant Year:	**2/ 3 /4**	Semester:	**ODD**	No. of Students Registered :	**50**
Venue:	**Seminar Hall, ,Ground Floor, SBECW**				

Outcome of Value Added Course (VAC):At the end of Course ,Students can able to

- Design the system meeting the specifications
- Design the data path and the controller(s) to implement the functionality.
- Develop Verilog based programs and simulate digital circuits.
- Analyze a VHDL code and infer what circuit a synthesis tool might generate out of a code.
- Implement digital circuits in Xilinx FPGA processor using Hardware description Language experimentally.
- Design and code to exploit the architectural features of FPGA.

No. of students successfully completed the VAC course is **50 Students** based on the following Assessment process.

Assessment Process

- Students securing **more than 60% on total score** and secured more than **75%** in attendance is eligible to receive the certificate for the VAC course conducted
- Total Score = (0.5 *Attendance in VAC out of 100 percentage + 0.5 *Test mark in VAC out of 100 marks)

VAC Coordinator **HoD/ ECE** **Principal** 26/6/18

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MARIA ACADEMY

CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. ATCHAYA.G, III YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

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Ganesan
RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU .
MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM

MARIA ACADEMY

CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. ABIRAMI.S, II YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

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Ganesan
RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU .
MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM

MARIA ACADEMY

CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. VENNILA .K, IV YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Name of the Student : **Year/Sem:**

AU Register Number:

Value Added Course on "**Digital System Design with Xilinx**"

MCQ QUESTIONS (25X1 = 25 Marks)

1. Which of the following options comes under the non – saturated logic family in Digital Electronics?
   a) Emitter – coupled Logic
   b) High-Threshold Logic
   c) Integrated – injection Logic
   d) Diode – Transistor Logic

2. Which characteristic of IC in Digital Circuits represents a function of the switching time of a particular transistor?
   a) Fan – out
   b) Fan – in
   c) Power dissipation
   d) Propagation delay

3. Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?
   a) Two 2 input AND gates
   b) Two 3 input AND gates
   c) Two 2 input OR gates
   d) Two 3 input OR gates

4. What must be used along with synchronous control inputs to trigger a change in the flip flop?
   a) 0
   b) 1
   c) Clock
   d) Previous output

5. What are the basic gates in MOS logic family?
   a) NAND and NOR
   b) AND and OR
   c) NAND and OR
   d) AND and NOR

6. Which of the following is only predefined physical literal in VHDL?
   a) Voltage
   b) Time
   c) Current
   d) Distance

7. Access types are similar to _____ in traditional programming languages.
   a) Pointers
   b) Arrays
   c) Structures
   d) Files

8. Which of the following is default delay in VHDL?
   a) Inertial delay
   b) Transport delay
   c) Delta delay
   d) Wire delay

9. Transport delay is a kind of _____
   a) Synthesis delay
   b) Simulation delay
   c) Inertial delay
   d) Wire delay

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10. A buffer with single input A and single output B has a delay of 20 nanosecond. If the value of input A changes after 10 ns from 0 to 1 and it changes again from 1 to 0 at 20 ns. At what time, the value of output B will be 1, if the transport delay model is used?
    a) 20 ns
    b) 30 ns
    c) 40 ns
    d) Output will remain zero

11. The process used for implementation of sequential logic in VHDL is called _____ process.
    a) Sequential process
    b) Combinational process
    c) Clocked process
    d) Unlocked process

12. A user doesn't want to use the IF statement for detecting clock edge. It is possible to do the same by using any other keyword in VHDL.
    a) True
    b) False

13. PLA contains _____
    a) AND and OR arrays
    b) NAND and OR arrays
    c) NOT and AND arrays
    d) NOR and OR arrays

14. A PLA is similar to a ROM in concept except that _____
    a) It hasn't capability to read only variables
    b) It hasn't capability to read or write operation
    c) It doesn't provide full decoding to the
    d) It hasn't capability to write only

15. The complex programmable logic device contains several PLD blocks and ____
    a) A language compiler
    b) AND/OR arrays
    c) Global interconnection matrix
    d) Field-programmable switches

16. Which type of device FPGA are?
    a) SLD
    b) SROM
    c) EPROM
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17. In FPGA, vertical and horizontal directions are separated by _____
    a) A line
    b) A channel
    c) A strobe
    d) A flip-flop

18. In a digital clock application, the basic frequency must be divided down as ___
    a) 1 Hz
    b) 60 Hz
    c) 100 Hz
    d) 1000 Hz

19. Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?
    a) Simulation
    b) Optimization
    c) Synthesis
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20. An Antifuse programming technology is predominantly associated with _____.
    a) SPLDs
    b) FPGAs
    c) CPLDs
    d) All of the above

21. In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?
    a) Floor planning
    b) Placement & Routing
    c) Testing
    d) Extraction

22. In logic synthesis, _____ is an EDIF that gives the description of logic cells & their inter connections.
    a) Netlist
    b) Shitlist
    c) Checklist
    d) Dualist

23. Which among the following operation/s is/are executed in physical design or layout synthesis stage?
    a) Placement of logic functions in optimized circuit in target chip
    b) Interconnection of components in the chip
    c) Both a and b
    d) None of the above

24. In synthesis flow, which stage/s is/are responsible for converting an un optimized boolean description to PLA format?
    a) Flattening
    b) Translation
    c) Optimization
    d) All of the above

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    a) Front end
    b)Back end
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    d) None of the above

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

Value Added Course on "**Digital System Design with Xilinx**"

MCQ ANSWER KEY

1	A	**6**	B	**11**	C	**16**	D	**21**	D
2	D	**7**	A	**12**	A	**17**	B	**22**	A
3	A	**8**	A	**13**	A	**18**	A	**23**	C
4	C	**9**	D	**14**	C	**19**	C	**24**	A
5	A	**10**	B	**15**	C	**20**	B	**25**	B

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Name of the Student : C. Karya **Year/Sem:** II / III

AU Register Number: 912617106011

Value Added Course on "**Digital System Design with Xilinx**"

MCQ QUESTIONS (25X1 = 25 Marks)

1. Which of the following options comes under the non – saturated logic family in Digital Electronics?
   (a) Emitter – coupled Logic
   b) High-Threshold Logic
   c) Integrated – injection Logic
   d) Diode – Transistor Logic

2. Which characteristic of IC in Digital Circuits represents a function of the switching time of a particular transistor?
   a) Fan – out
   b) Fan – in
   c) Power dissipation
   (d) Propagation delay

3. Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?
   (a) Two 2 input AND gates
   b) Two 3 input AND gates
   c) Two 2 input OR gates
   d) Two 3 input OR gates

4. What must be used along with synchronous control inputs to trigger a change in the flip flop?
   a) 0
   b) 1
   (c) Clock
   d) Previous output

5. What are the basic gates in MOS logic family?
   (a) NAND and NOR
   b) AND and OR
   c) NAND and OR
   d) AND and NOR

6. Which of the following is only predefined physical literal in VHDL?
   a) Voltage
   (b) Time
   c) Current
   d) Distance

7. Access types are similar to _____ in traditional programming languages.
   (a) Pointers
   b) Arrays
   c) Structures
   d) Files

8. Which of the following is default delay in VHDL?
   (a) Inertial delay
   b) Transport delay
   c) Delta delay
   d) Wire delay

9. Transport delay is a kind of _____
   a) Synthesis delay
   (b) Simulation delay
   c) Inertial delay
   d) Wire delay

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10. A buffer with single input A and single output B has a delay of 20 nanosecond. If the value of input A changes after 10 ns from 0 to 1 and it changes again from 1 to 0 at 20 ns. At what time, the value of output B will be 1, if the transport delay model is used?
    a) 20 ns
    b) 30 ns
    c) 40 ns
    d) Output will remain zero

11. The process used for implementation of sequential logic in VHDL is called _____ process.
    a) Sequential process
    b) Combinational process
    c) Clocked process
    d) Unlocked process

12. A user doesn't want to use the IF statement for detecting clock edge. It is possible to do the same by using any other keyword in VHDL.
    a) True
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13. PLA contains _____
    a) AND and OR arrays
    b) NAND and OR arrays
    c) NOT and AND arrays
    d) NOR and OR arrays

14. A PLA is similar to a ROM in concept except that _____
    a) It hasn't capability to read only variables
    b) It hasn't capability to read or write operation
    c) It doesn't provide full decoding to the
    d) It hasn't capability to write only

15. The complex programmable logic device contains several PLD blocks and ____
    a) A language compiler
    b) AND/OR arrays
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Name of the Student : A. Dharaniya **Year/Sem:** III / V

AU Register Number: 912616106005

Value Added Course on "**Digital System Design with Xilinx**"

MCQ QUESTIONS (25X1 = 25 Marks)

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Name of the Student : T. MEENAL **Year/Sem:** IV / VII

AU Register Number: 912615106010

Value Added Course on "**Digital System Design with Xilinx**"

MCQ QUESTIONS (25X1 = 25 Marks)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONENGINEERING

ACADEMIC YEAR ODD SEMESTER (2018-2019)

MARK SHEET FOR VALUE ADDED COURSE- "DIGITAL SYSTEM DESIGN WITH XILINX"

S.NO	REGISTER NUMBER	NAME	YEAR & BRANCH	Attendance (A)		VAC –MCQ TEST (B)		OVERALL MARK(100) (50% of A + 50% of B)
				No.of Sessions Attented	Marks (100)	No.of Correct Answer	Marks (100)	
1	912617106001	ABIRAMI.S	II /ECE	10	100	22	88	94
2	912617106002	ABISHEKA.S	II /ECE	10	100	23	92	96
3	912617106003	ATSHAYA.R	II /ECE	9	90	21	84	87
4	912617106004	BAVADHARANI.A	II /ECE	9	90	20	80	85
5	912617106005	BHUVANESHWARI.B	II /ECE	10	100	19	76	88
6	912617106006	DHIVYA.L	II /ECE	10	100	20	80	90
7	912617106007	GOWSALYA.D	II /ECE	10	100	21	84	92
8	912617106009	INDHUMATHI.S	II /ECE	9	90	19	76	83
9	912617106010	KANIMOZHI.D	II /ECE	10	100	18	72	86
10	912617106011	KAVYA.C	II /ECE	10	100	22	88	94
11	912617106012	KEERTHANA.G	II /ECE	10	100	20	80	90

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12	912617106013	MAHESHWARI.G	II /ECE	10	100	19	76	88
13	912617106014	MANOHARI.M	II /ECE	10	100	18	72	86
14	912617106015	MARAGATHALAKSHMI.S	II /ECE	8	80	20	80	80
15	912617106017	SAFRIN NISHA.S	II /ECE	10	100	20	80	90
16	912617106018	SUBASHINI.M	II /ECE	10	100	18	72	86
17	912617106019	SUBASHINI.T	II /ECE	8	80	19	76	78
18	912617106020	VINTHIYA.R	II /ECE	10	100	22	88	94
19	912616106001	ABINAYA.R	III /ECE	10	100	19	76	88
20	912616106002	AGALYA.A	III /ECE	8	80	18	72	76
21	912616106003	ATCHAYA.G	III /ECE	10	100	19	76	88
22	912616106004	DEEPA.N	III /ECE	10	100	22	88	94
23	912616106005	DHARANIYA.A	III /ECE	9	90	18	72	81
24	912616106006	JEEVITHA.U	III /ECE	10	100	19	76	88
25	912616106007	MAHESWARI.V	III /ECE	8	80	21	84	82
26	912616106008	PAZHANIYAMMAL.R	III /ECE	10	100	23	92	96
27	912616106009	PRIYANKA.E	III /ECE	10	100	21	84	92
28	912616106010	ROJA.A	III /ECE	10	100	23	92	96
29	912616106011	SHANMUGAPRIYA.R	III /ECE	10	100	19	76	88
30	912616106012	SHIYAMALA.E	III /ECE	10	100	19	76	88
31	912616106013	SIVA BHARATHI.P	III /ECE	10	100	18	72	86
32	912616106014	SIVARUBINI.S	III /ECE	10	100	23	82	91

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33	912616106015	THENMOZHI.A	III /ECE	8	80	18	72	76
34	912616106016	VINCY.A	III /ECE	10	100	18	72	86
35	912616106302	SANKAVI M	III /ECE	10	100	19	76	88
36	912615106001	AARTHI .M	IV/ECE	9	90	18	72	81
37	912615106002	ABIRAMI .C	IV/ECE	10	100	20	80	90
38	912615106004	AKILA .S	IV/ECE	10	100	19	76	88
39	912615106005	ARTHI .M	IV/ECE	10	100	18	72	86
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41	912615106007	DIVYABHARATHI .S	IV/ECE	10	100	19	76	88
42	912615106008	JAGADESWARI .K	IV/ECE	10	100	17	68	84
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44	912615106010	MEENAL .T	IV/ECE	10	100	21	84	92
45	912615106012	SARGUNAVALLI .C	IV/ECE	8	80	20	80	80
46	912615106013	THENMOZHI .K	IV/ECE	10	100	15	60	80
47	912615106014	VENNILA .K	IV/ECE	10	100	22	88	94
48	912615106301	MANIMEGALAI .S	IV/ECE	9	90	19	76	83
49	912615106701	SARADHA .S	IV/ECE	10	100	23	92	96
50	912615106702	KAVIYA. S	IV/ECE	10	100	20	80	90

VAC Coordinator

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HoD/ ECE

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