SRI BHARATHI

ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai)

Kaikkurichi, Pudukkottai -622 303

www.sbec.edu.in

NAAC DOCUMENTS

Quality Indicator Frame Work

Criterion – 1

CURRICULAR ASPECTS

Submitted by

IQAC

Internal Quality Assurance Cell

Sri Bharathi Engineering College for Women

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)

Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Criterion 1	Curricular Aspects	100

1.1 Curricular Planning and Implementation(20)

1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

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SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai-25)
Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

PREFACE OF THE COURSE FILE

Batch : **2018-2022**

Academic Year : **2019-2020 / ODD**

Program : **ELECTRICAL AND ELECTRONICS ENGINEERING**

Year & Semester : **2nd Year / 3rd Semester**

Course Code : **EE 8351** NBA Course Code: **C202**

Name of the Course : **Digital Logic Circuits**

Faculty in-charge : R.RAGADHARSHINI AP / **EEE**

R. Ragadharshini

Signature of the Faculty Incharge

HoD / EEE

Dr. S.THILAGAVATHI M.E.,Ph.D.,
PRINCIPAL
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Kaikkurichi - 622 303, Pudukkottai Dt.

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

REVIEW OF COURSE FILE

(to be pasted on the inner side of the file-backside).(#-State Yes/No.)

S.N	Details Date:	R-I-*	R-II-*&	R-III-*&	R-IV-*&$	R-V-*&$@
1.	Preface of the course file	Yes				
2.	Vision, Mission, PEOs, POs, PSOs, Blooms taxonomy	Yes				
3.	Subject handlers of yesteryears	Yes				
4.	Timetable/Workload of the staff – Distribution of teaching load – Roles and Responsibilities	Yes				
5.	Syllabus signed by staff & HoD	Yes				
6.	Lecture Schedule signed by staff & HoD	Yes				
7.	Course Committee meeting circular and minutes	NA				
8.	Identification of Curricular gap and Content Beyond the syllabus	Yes				
9.	Self-study topics	Yes				
10.	Previous AU Question papers	Yes				
11.	Unit wise Q&A and Objective type questions	Yes				
12.	Unit wise course material	Yes				
13.	Assignment question paper with sample answer sheets and mark entry		Yes			
14.	Tutorial question paper with key and mark entry		Yes			
15.	Class test/IA test Q Paper with Key, sample answer papers and mark entry		Yes			
16.	IA Test- result analysis-CAP-evidence-root cause analysis.		Yes			
17.	Retest –Q paper-Attendance-marks			Yes		
18.	AU Web portal entry sheet			Yes		
19.	Very poor performance in first two tests-action taken.-communication to parents-evidence			Yes		
20.	Absence for two tests-action taken-communication to parents-evidence.			–		
21.	Indiscipline of student reported, if any			–		
22.	Special class/coaching class/remedial class/attendance-CAP			Yes		
23.	Conduct of Seminar, Quizzes - proof			Yes		
24.	Content beyond the syllabus - proof			Yes		
25.	Student feedback on faculty				Yes	
26.	Course end survey				Yes	
27.	Internal Assessment sheet				Yes	
28.	AU question paper with students feedback				Yes	
29.	Discrepancy of the question paper and correspondence, if any				Yes	
30.	AU result analysis-Details of arrear students.					Yes
31.	AU grade sheet					Yes
32.	CO – PO & PSO attainment sheet					Yes
	Signature of Course handling faculty	R.R	R.R	R.R	R.R	R.R
	Signature of HoD					

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DEPARTMENT OF EEE

INDIVIDUAL STAFF WORKLOAD (2019-2020) ODD SEMESTER

S. NO.	NAME OF THE STAFF	SUBJECTS HANDLED	YEAR & DEPT	HOURS ALLOCATED	TOTAL HOURS
1.	Mrs.A.PRIMROSE	**OMD551** –Basics of Bionedical Instrumentation	III EEE & ECE	5	11
		MG6851- Principle of Management	IV EEE	6	
2.	Mrs. SUSILADEVI.S	**EE6701**-High Voltage Engineering	IV EEE	6	14
		ORO551-Renewable Energy Sources	III/CIVL	5	
		EE6711 –Power System Simulation Laboratory	IV EEE	3	
3.	Mr. SATHYARAJ.J	**EE8501**-Power System Analysis	III EEE	5	13
		EE6703-Special Electrical Machines	IV EEE	5	
		EE8311-Electrical Machines-I Laboratory	II EEE	3	
4.	Ms.K.A.MUTHULAKSHMI	**EE8391**-Electromagnetic Theory	II EEE	5	10
		EC8353-Electron Devices and Circuits	III EEE	5	
5.	Mrs.R.AKILANDESWARI	**EC8391**-Control System Engineering	II ECE	5	13
		EE6702- Protection and Switchgear	IV EEE	5	
		EE8511- Control and Instrumentation Laboratory	III EEE	3	
6.	Ms.S.DEVAKI	**EE8301**-Electrical Machines-I	II EEE	6	11
		EE8511- Control and Instrumentation Laboratory	III EEE	3	
		EE6712- Comprehension	IV EEE	2	
7.	Ms.M.ABIRAMI	**EE8852**- Power Electonics	III EEE	5	10
		OMD551 –Basics of Bionedical Instrumentation	III CSE	5	

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8.	Mrs.PL.KAVITHA	**EE6008**- Microcontroller Based System Design	**IV EEE**	**5**	**10**
		ME8792- Power Plant Engineering	**II EEE**	**5**	
9.	Mrs. R.RAGADHARSHINI	**EE6004**- Flexible AC Transmission Systems	**IV EEE**	**5**	**11**
		EE8351- Digital Logic Circuits	**II EEE**	**6**	

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE PLAN

Subject code: EE 8351	**Branch/Year/Sem: B.E EEE/II/III**
Subject Name: DIGITAL LOGIC CIRCUITS	**Batch: 2018-2022**
Staff Name: R.RAGADHARSHINI	**Academic year: 2019-2020**

COURSE OBJECTIVE

- To study various number systems and simplify the logical expressions using Boolean functions.
- To study combinational circuits.
- To comprehend simulation using software package.
- To design various synchronous and asynchronous circuits.
- To introduce asynchronous sequential circuits and PLDs.
- To introduce digital simulation for development of application oriented logic circuits.

TEXT BOOK:

T1. James W. Bignel, Digital Electronics, Cengage learning, 5th Edition, 2007.
T2. Morris Mano.M, 'Digital Logic and Computer Design', Prentice Hall of India, 3rdEdition, 2005.
T3. Comer "Digital Logic & State Machine Design, Oxford, 2012.

REFERENCES:

R1. Mandal, "Digital Electronics Principles & Application, McGraw Hill Edu, 2013.
R2. William Keitz, Digital Electronics-A Practical Approach with VHDL, Pearson, 2013.
R3. Thomas L.Floyd, 'Digital Fundamentals', 11th edition, Pearson Education, 2015.
R4. Charles H.Roth, Jr, Lizy Lizy Kurian John, 'Digital System Design using VHDL, Cengage,2013.
R5. D.P.Kothari,J.S.Dhillon, 'Digital circuits and Design',Pearson Education, 2016.

WEB RESOURCES

W1: https://drive.google.com/file/d/1k4smOjN2KroypS6DJFWobYNSRriReHsR/view
W2: https://drive.google.com/file/d/1Srb2uBfYS3iy_h0Z1rSXgp8BJ3mQwU6d/view
W3: https://ocw.mit.edu/courses/6-973-communication-system-design-spring-2006/44d1cff68d0f994cca25442de3

TEACHING METHODOLOGIES:

- BB - BLACK BOARD
- PPT - POWER POINT PRESENTATION

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EE8351	DIGITAL LOGIC CIRCUITS	L	T	P	C
		2	2	0	3

UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES **6+6**

Review of number systems, binary codes, error detection, and correction codes (Parity and Hamming code) - Digital Logic Families -comparison of RTL, DTL, TTL, ECL and MOS families - operation, characteristics of digital logic family.

UNIT II COMBINATIONAL CIRCUITS **6+6**

Combinational logic - representation of logic functions-SOP and POS forms, K-map representations - minimization using K maps - simplification and implementation of combinational logic – multiplexers and de multiplexers - code converters, adders, subtractors, Encoders and Decoders.

UNIT IIISYNCHRONOUS SEQUENTIAL CIRCUITS **6+6**

Sequential logic- SR, JK, D and T flip flops - level triggering and edge triggering - counters - asynchronous and synchronous type - Modulo counters - Shift registers - design of synchronous sequential circuits – Moore and Mealy models- Counters, state diagram; state reduction; state assignment.

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABILITY LOGIC DEVICES **6+6**

Asynchronous sequential logic Circuits-Transition stability, flow stability-race conditions, hazards &errors in digital circuits; analysis of asynchronous sequential logic circuits-introduction to Programmability Logic Devices: PROM – PLA –PAL, CPLD-FPGA.

UNIT V VHDL **6+6**

RTL Design – combinational logic – Sequential circuit – Operators – Introduction to Packages – Subprograms – Test bench. (Simulation /Tutorial Examples: adders, counters, flip flops, Multiplexers & De multiplexers).

TOTAL: 60 PERIODS

R.R

Faculty Incharge

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Topic No	Topic Name	Books For reference	Page No	Teaching Methodology	No of periods required	Cumulative periods
UNIT I	**NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES**					**(6+6)**
1.	Number system	T2	1	BB	1	1
2.	error detection, corrections code(Parity and Hamming code)	T2	299	BB	2	3
3.	Digital Logic Families	T2	399	PPT	1	4
4.	comparison of RTL, DTL, TTL, ECL and MOS families	T2	409	PPT	3	7
5.	operation	T2	412	BB	2	9
6.	characteristics of digital logic family	T2	422	BB	3	12
7.	Tutorial	T2	299	BB	1	13
LEARNING OUTCOME: **At the end of unit , the students will be able to** • Know the fundamentals of Number system. • Understand the concept of Boolean Algebra. • Define the types of digital logic families.						
UNIT II	**COMBINATIONAL CIRCUITS**					**(6+6)**
8.	Combinational logic	T2	114	BB	2	15
9.	representation of logic functions	T2	115	BB		
10.	SOP and POS forms	T2	84	BB	2	17
11.	K-map representations	T2	72	BB		
12.	minimization using K maps	T2	73	BB	2	19
13.	simplification and implementation of combinational logic	T2	78	BB	1	20
14.	multiplexers and de multiplexers	T2	173	BB	1	21
15.	code converters	T2	124	PPT	1	22
16.	adders	T2	116	BB	1	23
17.	subtractors	T2	121	BB	1	24
18.	Encoders and Decoders	T2	166	BB	1	25
19.	Tutorial	T2	72	BB	1	26

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LEARNING OUTCOME:

At the end of unit , the students will be able to

- Understand the concept of combinational logic circuits.
- Analyze and implement the combinational logic circuits.

UNIT – III	SYNCHRONOUS SEQUENTIAL CIRCUITS					(6+6)
20.	Sequential logic	T2	202	BB	1	27
21.	SR, JK, D and T flip flops	T2	204	BB	2	29
22.	level triggering and edge triggering	T2	210	BB	1	30
23.	counters	T2	247	BB	1	31
24.	asynchronous and synchronous type	T2	202	BB		
25.	Modulo counters	T2	272	BB	1	32
26.	Shift registers	T2	264	PPT	1	33
27.	design of synchronous sequential circuits	T2	236	BB	1	34
28.	Moore and Mealy models	T2	218	BB	2	36
29.	Counters, state diagram; state reduction; state assignment	T2	218	BB	2	38
30	Tutorial	T2	204	BB	1	39

LEARNING OUTCOME:

At the end of unit , the students will be able to

- Understand the concept of Sequential logic circuits.
- Study about flip-flops.
- Design and analyze the synchronous sequential circuits.

UNIT IV	ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGAMMABILITY LOGIC DEVICES					(6+6)
31.	Asynchronous sequential logic Circuits	T2	341	BB	1	40
32.	Transition stability	T2	366	BB	1	41
33.	flow stability	T2	366	BB	1	42
34.	race conditions	T2	374	BB		
35.	hazards &errors in digital circuits	T2	379	BB	1	43
36.	analysis of asynchronous sequential logic circuits	T2	343	BB	1	44
37.	introduction to Programmability Logic Devices: PROM	T2	180	BB	1	45
38.	PLA	T2	187	BB	1	46
39.	PAL	T2	192	BB		
40.	CPLD	R2	628	PPT	1	47
41.	FPGA	R2	628	PPT	1	48
42.	ASIC(CBS)	W3		PPT	2	50
43.	Tutorial	T2	187	BB	1	51

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LEARNING OUTCOME:

At the end of unit , the students will be able to

- Design and analyze the Asynchronous sequential circuits.
- Understand the concept of programmable logic devices.

UNIT V VHDL						(6+6)
44.	RTL Design	R2	597	PPT	2	53
45.	combinational logic	R2	599	BB	2	55
46.	Sequential circuit	R2	599	BB	2	57
47.	Operators	R2	599	BB	1	58
48.	Introduction to Packages	R2	602	BB	1	59
49.	Subprograms	R2	602	BB	1	60
50.	Test bench(Simulation /Tutorial Examples: adders, counters, flip flops, Multiplexers & De multiplexers)	R2	605	BB	5	65

LEARNING OUTCOME:

At the end of unit , the students will be able to

- Understand the RTL design of FPGA.
- Know about the VHDL.
- Program for combinational and sequential logic circuits.

COURSE OUTCOME

At the end of the course, the student should be able to:

- C202.1: Comprehend various number systems and simplify the logical expressions using Boolean functions.
- C202.2: Explain about the combinational circuits.
- C202.3: Design various synchronous sequential circuits.
- C202.4: Develop the asynchronous sequential circuits.
- C202.5: Describe about PLDs and FPGA.
- C202.6: Demonstrate the digital simulation for development of application oriented logic circuits.

CONTENT BEYOND THE SYLLABUS

ASIC

ASSESSMENT DETAILS

ASSESMENT NUMBER	I	II	III
UNIT	1st & 2nd (Half) Units	2nd (Half) & 3rd units	4th & 5th units

ASSIGNMENT DETAILS	I	II	III
DATE OF SUBMISSION	19.07.2019	21.08.2019	25.09.2019

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ASSIGNMENT NUMBER	UNIT	DESCRIPTIVE QUESTIONS/TOPIC
1	I,II(Half)	COMPARISON BETWEEN DIGITAL LOGIC FAMILIES, K-MAP PROBLEMS
2	II(Half),III	SOP & POS, ENCODER & DECODER, CONVERSION OF FLIP FLOP
3	IV,V	STEPS FOR ASYNCHRONOUS SEQUENTIAL CIRCUITS, PROGRAMS(FULL ADDER – 3MODEL)

PREPARED BY

Mrs.R.RAGADHARSHINI, AP/EEE

VERIFIED BY

HOD/EEE

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APPROVED BY 26/04/19

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Identification of Curricular Gap & Content Beyond Syllabus(CBS)

Name of the Faculty :R.RAGADHARSHINI **Course Code & Name:EE8351 & Digital Logic Circuits**

Degree & Program: B.E. /EEE **Semester & Section: III** **Academic Year: 2019 -2020 /ODD**

I. Mapping of Course Outcomes with POs & PSOs.(before CBS)

Table.1 Mapping of COs, C, PSOs with POs - before CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C202.1	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.2	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.3	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.4	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.5	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.6	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1

II. Identification of content beyond syllabus.

Table.2 Identification of content beyond syllabus

Details of Content Beyond Syllabus(CBS) added	POs strengthened/ vacant filled	CO/Unit
ASIC	PO6(1)&PO9(1)/ Vacant filled	C202.6/filled

III. Mapping of Course Outcomes with POs & PSOs. (After CBS)

Table.3 Mapping of COs, C, PSOs with POs- after CBS.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C202.1	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.2	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.3	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.4	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.5	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.6	2	2	1	1	1	*2	-	-	*2	1	-	1	2	-	1
C202	2	2	1	1	1	*2	-	-	*2	1	-	1	2	-	1

R. Raghavi
Signature of the Faculty

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Assignment Question Paper

Assignment – 03			Date of Issue:	20.09.2019	Marks	20
Course code	EE8351	Course Title	Digital Logic Circuits			
Year	II	Semester	III	Date of Submission:	25.09.2019	

Q.No	Questions	CO
1	Draw a PLA circuit to implement the functions F 1 =AB'+AC+A'BC' and F 2 = (AC+BC)'.	C202.5
2	Write the VHDL program for full adder in all three types of modeling?	C202.6

R. Raghli

Name and Signature of the Faculty Incharge

(Mrs. R. RAGHADHARSHINI)

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Assignment Answer Sheet

Name of the Student : NISHA K

AU Register Number: 912618105005

Assignment – 03			Date of Issue:	20.09.2019	Marks	20
Course code	EE8351	Course Title	Digital Logic Circuits			
Year	II	Semester	III	Date of Submission:	25.09.2019	

Q.No	Questions	CO
1	Draw a PLA circuit to implement the functions F 1 =AB'+AC+A'BC' and F 2 = (AC+BC)'.	C202.5
2	Write the VHDL program for full adder in all three types of modelling?	C202.6

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Content Quality	16	16
Presentation Quality	2	01
Timely submission	2	01
Total marks	20	18

R. Raghavi

Name and Signature of the Faculty Incharge

(Mrs. R. RAGHADHARSHINI)

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Tutorial Question Paper

Tutorial – 02			Date of Issue:	01.08.2019	Marks	30
Course code	EE8351	Course Title	Digital Logic Circuits			
Year	II	Semester/Section	III	Date of Submission:	06.08.2019	

Q. No	Questions	CO
1	Implement the following Boolean function using K-map f(A,B,C)=A'.B'.C'+A'B'C'+A'BC'+A'B'C	C202.2
2	Convert the given expression into standard sop form also find minterms. i)f(A,B,C)=AC+AB+AC' ii)f(A,B,C)=A+B	C202.2
3	Reduce the following function using tabulation method and verify using K map and draw the logic diagram. F(A,B,C)=A'B'C'+A'BC'+AB'C'+ABC'+ABC	C202.2

R. Raghadharshini

Name and Signature of the Faculty Incharge

(MRS. R. RAGHADHARSHINI)

HoD/EEE

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SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN
KAIKKURICHI,
PUDUKKOTTAI - 622 303.

Dr. S.THILAGAVATHI M.E.,Ph.D.,
PRINCIPAL
SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN
Kaikkurchi - 622 303, Pudukkottai Dt.

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai-25)
Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Tutorial Answer Sheet

Name of the Student : RAMANA R

AU Register Number: 912618105006

Tutorial – 02				Date of Issue:	01.08.2019	Marks	30
Course code	EE8351	Course Title	Digital Logic Circuits				
Year	II	Semester	III	Date of Submission:	06.08.2019		

Q.No	Questions	CO
1	Implement the following Boolean function using K-map f(A,B,C)=A'.B'.C'+A'B'C'+A'BC'+A'B'C	C202.2
2	Convert the given expression into standard sop form also find minterms. i)f(A,B,C)=AC+AB+AC' ii)f(A,B,C)=A+B	C202.2
3	Reduce the following function using tabulation method and verify using K map and draw the logic diagram. F(A,B,C)=A'B'C'+A'BC'+AB'C'+ABC'+ABC	C202.2

Mark Allocation

Rubrics	Marks Allocated	Marks obtained
Problem solving approach	20	18
Correctness of Answer	5	05
Timely submission	5	03
Total marks	30	26

R. Raghu

Name and Signature of the Faculty Incharge

(Mrs. R. RAGHADHARSHINI)

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IQAC Academic Audit Form

ACADEMIC YEAR: 2019-2020 ODD SEMESTER

Name of Department :	EEE	Year / Sem :	II/III	No. of Students Registered :	08
Details of Examination :	CT-1 / CT-2 / CT-3 / Model Test				

S.No.	Course Code	List of Reg.No Verified	Course Log Book Verified (Y / N)	Course File Verified (Y / N)	No of students passed	No of Absentees	No of Failures	Pass %	Remarks
1	MA8353	912618105007	Y	Y	6	–	2	75%	–
2	EE8351	912618105006	Y	Y	7	–	1	87.5%	–
3	EE8391	912618105004	Y	Y	8	–	–	100%	–
4	EE8301	912618105001	Y	Y	6	–	2	75%	–
5	ME8792	912618105002	Y	Y	7	–	1	87.5%	–
6	EC8353	912618105003	Y	Y	8	–	–	100%	–

Verified by

External Member Name and Signature:	P. Dennis Flora, [P. Dennis Flora, AP/CIVIL]
Internal Member Name and Signature:	J. Sathyaraj [J. SATHYARAJ, AP/EEE]

Overall Remarks:

Concentrate more on results for the subjects MA8353 & EE8301

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IQAC Coordinator

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Principal

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PUDUKKOTTAI DISTRICT

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENINEERING

STUDENT FEEDBACK ON FACULTY

S.NO.	DESCRIPTION	SCORED OUT OF 4	SCORED OUT OF 100
1.	The Syllabus coverage as prescribed by University.	3.88	97
2.	Technical knowledge of the teacher.	3.75	93.75
3.	Teacher's communication skill.	3.88	97
4.	Regularity in taking classes.	3.63	90.75
5.	Helping the Students in conducting the experiment through set of instructions and Demonstrations.	3.63	90.75
6.	Tendency of inviting opinion and questions on subject matter from students.	3.63	90.75
7.	Knowledge of the Teacher in latest development of field.	3.63	90.75
8.	Perfectness of Valuation.	3.75	93.75
OVERALL SCORE		3.72	93.06

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REPORT SHEET

S .NO	REG.NO	NAME	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
1.	912618105001	AARTHI G	4	4	4	3	3	4	4	4
2.	912618105002	AASHA R	4	4	4	4	4	4	3	4
3.	912618105003	AGARI S	4	4	3	3	4	4	4	3
4.	912618105004	JEEVITHA R	4	3	4	4	3	4	3	4
5.	912618105005	NISHA K	4	4	4	4	4	3	4	4
6.	912618105006	RAMANA R	4	3	4	3	4	4	3	3
7.	912618105007	SNEHA S	3	4	4	4	4	3	4	4
8.	912618105301	VINOTHINI V	4	4	4	4	3	3	4	4
		AVERAGE	**3.88**	**3.75**	**3.88**	**3.63**	**3.63**	**3.63**	**3.63**	**3.75**
		PERCENTAGE	**97**	**93.75**	**97**	**90.75**	**90.75**	**90.75**	**90.75**	**93.75**

EXCELLENT	VERY GOOD	GOOD	AVERAGE	POOR
4	3	2	1	0

Signature of the Faculty

HoD/EEE

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SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN
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Circular Date: 23-09-2019

The third cycle test will be conducted from 03.10.2019 to 18.10.2019 for the III, V & VII semester (II, III & IV year) students.

The following instructions are to be followed by the faculty members.

- Total marks for which the question paper to be set will be for 100 marks.
- It is the responsibility of the question paper setter to take the Xerox copies of the required number of question papers with the help of Ms. Anusha. G & Ms. Keerthana. P and it should be handed over to the Exam Coordinator Mr. J. Sathyaraj A.P/ EEE two days before their examination.
- The Exam Coordinators (exam cell) are requested to make necessary arrangements (hall arrangements, invigilation duty etc.,) for conducting the test.
- Faculty members are requested to handover the valued answer scripts to the students on or before 19.10.2019 and the class in-charges are requested to send the consolidated mark sheet along with the attendance percentage to the parents on or before 22-10-2019.

PRINCIPAL

Cc:

- All faculty
- Exam cell
- Office file

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Circular

Date: 23-09-2019

The third cycle test will be conducted from 03.10.2019 to 18.10.2019 for the III semester (II year) B.E/ B.Tech students for 100 marks as per the timetable given below. Students are directed to prepare well and score good marks.

Date	9.30 am -12.30 am (FN) – 1.15 pm to 4.15 pm (AN)
03.10.2019 (AN)	**CE8301** Strength of Materials I **(Civil)** **EE8301** Electrical Machines - I **(EEE)** **CS8392** Object Oriented Programming **(CSE)** **MA8352** Linear Algebra and Partial Differential Equations **(ECE)**
10.10.2019 (FN)	**MA8353** Transforms and Partial Differential Equations **(Civil, EEE)** **MA8351** Discrete Mathematics **(CSE)** **EC8352** Signals and Systems **(ECE)**
12.10.2019 (FN)	**CE8351** Surveying **(Civil)** **EE8351** Digital Logic Circuits **(EEE)** **CS8391** Data Structures **(CSE)** **EC8351** Electronic Circuits- I**(ECE)**
14.10.2019 (AN)	**CE8302** Fluid Mechanics **(Civil)** **ME8792** Power Plant Engineering **(EEE)** **EC8395** Communication Engineering **(CSE)** **EC8393** Fundamentals of Data Structures In C **(ECE)**
16.10.2019 (AN)	**CE8392** Engineering Geology**(Civil)** **EE8391** Electromagnetic Theory **(EEE)** **COACHING (CSE)** **EC8392** Digital Electronics **(ECE)**
18.10.2019 (AN)	**CE8391** Construction Materials **(CIVIL)** **EC8353** Electron Devices and Circuits **(EEE)** **CS8351** Digital Principles and System Design **(CSE)** **EC8391** Control Systems Engineering **(ECE)**

PRINCIPAL

23/9/19

Cc:

- All II year B.E / B.Tech Classes
- All faculty
- Exam cell
- Notice Board
- Office file

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Register Number:												

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Cycle Test - III			Date/Session	12.10.2019/FN	Marks	60
Course code	EE8351	Course Title	DIGITAL LOGIC CIRCUITS			
Regulation	2017	Duration	90 minutes	Academic Year	2019-2020	
Year	II	Semester	III	Department	EEE	

COURSE OUTCOMES

CO1:	Comprehend various number systems and simplify the logical expressions using Boolean functions.
CO2:	Explain about the combinational circuits.
CO3:	Design various synchronous sequential circuits.
CO4:	Develop the asynchronous sequential circuits.
CO5:	Describe about PLDs and FPGA.
CO6:	Demonstrate the digital simulation for development of application oriented logic circuits.

Q.No.	Question	CO	BTS
	PART A (Answer all the Questions 10 x 2 = 20 Marks)		
1	What is fundamental mode sequential circuit?	C202.4	K1
2	What is pulse mode circuit?	C202.4	K1
3	Draw the block diagram of asynchronous sequential circuit.	C202.4	K3
4	What is state equivalence theorem?	C202.4	K1
5	List the different techniques used for state assignment.	C202.4	K1
6	What is the structural gate-level modeling?	C202.5	K1
7	What is Switch-level modeling?	C202.5	K1
8	What are identifiers?	C202.5	K1
9	Give the different arithmetic operators?	C202.5	K1
10	What are the types of procedural assignments?	C202.5	K1
	PART B (Answer all the Questions 2 x 13 = 26 Marks)		
11a	Describe the steps involved in design of asynchronous sequential circuit in detail with an example.	C202.4	K2
	OR		
11b	i) Write program in HDL to design 2 bit up/down counter. ii) Write the HDL program for 2:1 multiplexer in Dataflow and Behavioural description.	C202.4	K2
12a	Write the VHDL program for 4 bit counter.	C202.5	K2
	OR		
12b	Explain the various modeling methods used in VHDL with an example.	C202.5	K2
	PART C (Answer all the Questions 1 x 14 = 14 Marks)		
13a	i)Draw the VLSI design flowchart used for IC design and fabrication. ii) Write down a VHDL code for 8:1 multiplexer.	C202.5	K2
	OR		
13b	i)Differentiate PAL and PLA implementations with the help of the same example $F_2(a,b,c) = \Sigma(0,1,3,4,6,7)$. ii) Design a Modulo-6 asynchronous binary up-counter	C202.5	K2

R.R 10/10/19

Course Faculty

(Name /Sign / Date)

(Mrs. R. RAGADHARSHINI)

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10/10/19

HoD

(Name /Sign / Date)

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KAIKKURICHI.

EE8351 - Digital logic Circuits

Cycle Test - III

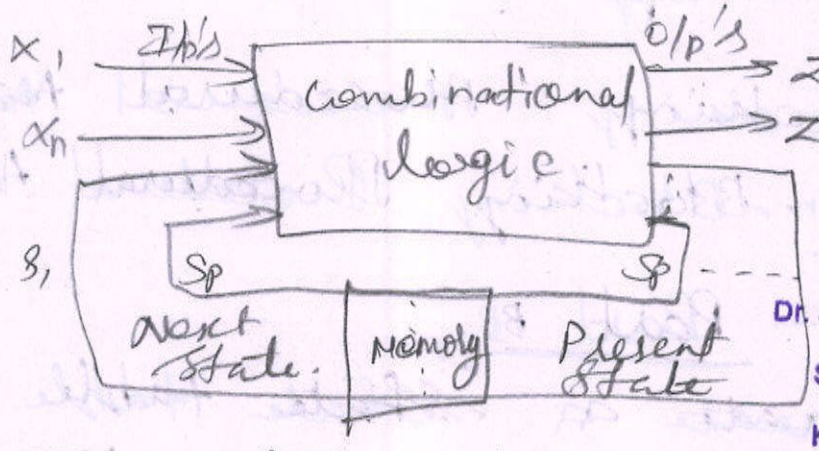
Key Answer

Academic year (2019-20) ODD SEM

1. * Input Variables changes if the Circuit is Stable
   * Inputs are levels, not pulses.
   * Only one input can change at a given time.

2. * Input are pulses.
   * Widths of pulses are long for Circuit to respond to the input.
   * Pulse width must not be so long that it is still present after the new state is reached.

3.



4. Two states in a sequential networks are said to be equivalent if we cannot tell them apart

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5. (1) Row Matching
(2) Implication charts.
(3) Successive Partitioning

6. It is virtually the lowest level of abstraction because the switch-level abstraction is rarely used. It is used to implement the lowest level modules in a design.

7. It is a recently developed design and analysis methodology for MOS VLSI Circuits.

8. Identifiers are the names you supply for variables, types, functio and labels in your program.

9. '+' - addition '-' - Subtraction
'*' - Multiplication '/' - Division.

10. 1. Blocking Procedural Assignment
2. Non-Blocking Procedural Assignmen

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Part B

11. a) Create a State table or State diagram from the given problem Statement.

2. Create a new reduced State table by removing all the redundant States
3. Create the transition table.
4. Write the excitation and output Boolean equations and simplify them.
5. Draw the logic diagram. (13m)

11.b)(i). Module my_counter (clk, reset, c_out);
input clk, reset; (8m)
output [1:0] c_out;
reg [1:0] c_up = 2'b00;
always @ (posedge clk, negedge reset)
begin
if (!reset)
c_up <= 2'b00;
else
c_up <= c_up + 2'b01;
end
assign c_out = c_up;
Endmodule;

12 a) i) Entity mux 8to1 is (13m)
Port (s: in bit_vector (2 downto 0);
d: in bit_vector (7 downto 0);
y: out bit);
End mux 8to1;

architecture Equation of mux8to1 is
begin
With s Select
Y <= d(0) when '000',
d(1) when '001',
d(2) when '010',
d(3) when '011'; d(4) when '100',
d(5) when '101'; d(6) when '110',
d(7) when 'others';

12)a) Module counter (clk, reset, up_down, l, d, c);
input clk, reset, l, up_down;
input [3:0] d;
Output reg [3:0] c;
the clock
always @ (posedge clk)
begin
if (reset) c<= 0;
else if (l) c <= d;
else if (up_down) c <= c+1;
else c <= c-1;
end
Endmodule;

12 b). 1. Data flow [Example] 4 m
2. Structural. " 5 m

13)a)(i)

System Specification
↓
Architectural Design
↓
Functional Design & Logic Design
↓
Circuit Design
↓
Physical Design
↓
Physical Verf & Sign off
↓
Fabrication
↓
Packaging & Testing
↓
Chip

Physical Design →
- Partitioning
- Chip planning
- Placement
- Clock Tree Synthesis
- Signal Routing
- Timing Closure

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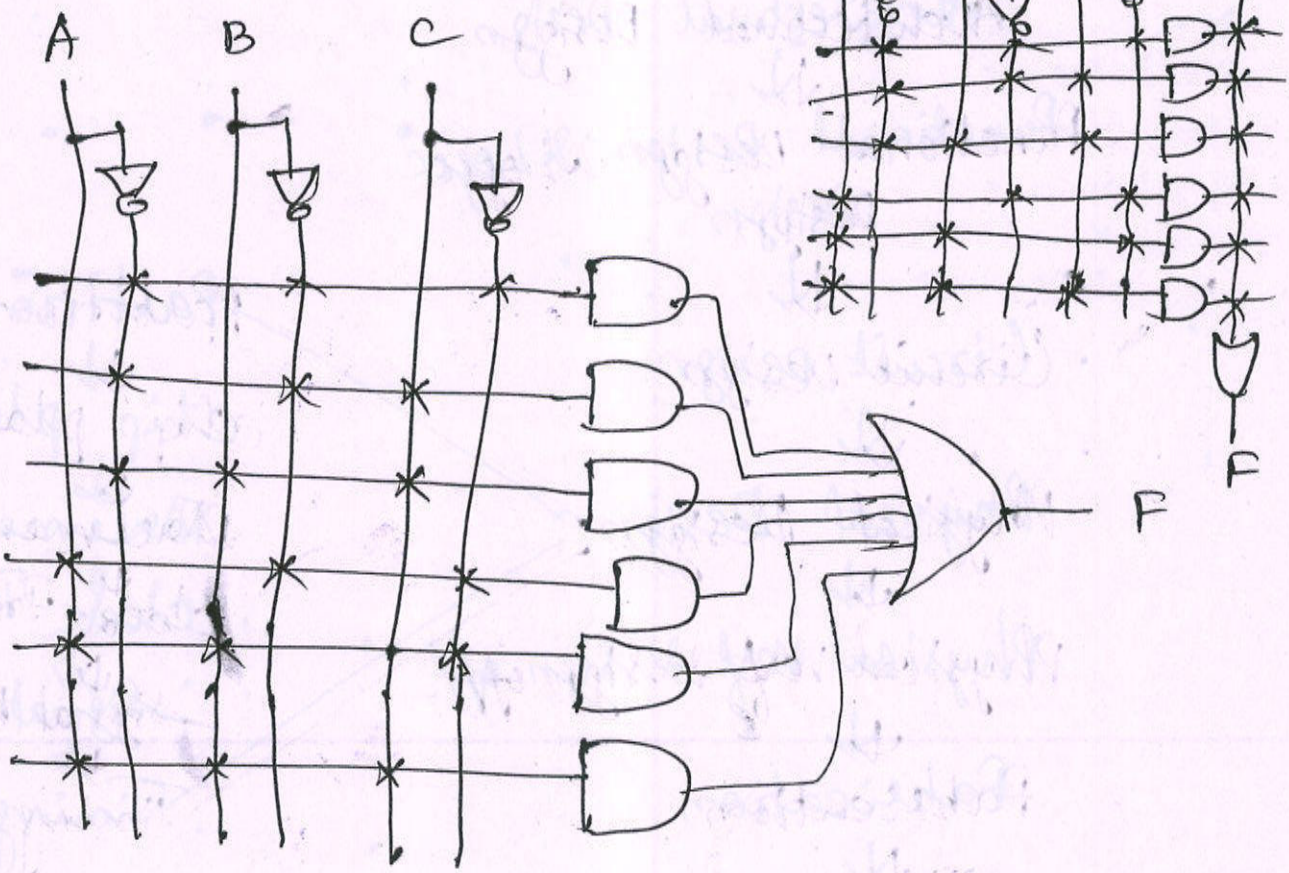
11)b)(i)

```
Entity mux2 IS.
  Port (S, W : IN std_logic;
        f : OUT std_logic);
End mux2;
Architecture structure of mux2 is
  Signal m : std_logic;
Begin
  mapping : mux2 Port Map
      (w(0), w(1), s(0), m(0));
End structure;
```

(3) B)(i) PAL

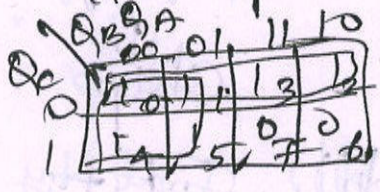


PLA

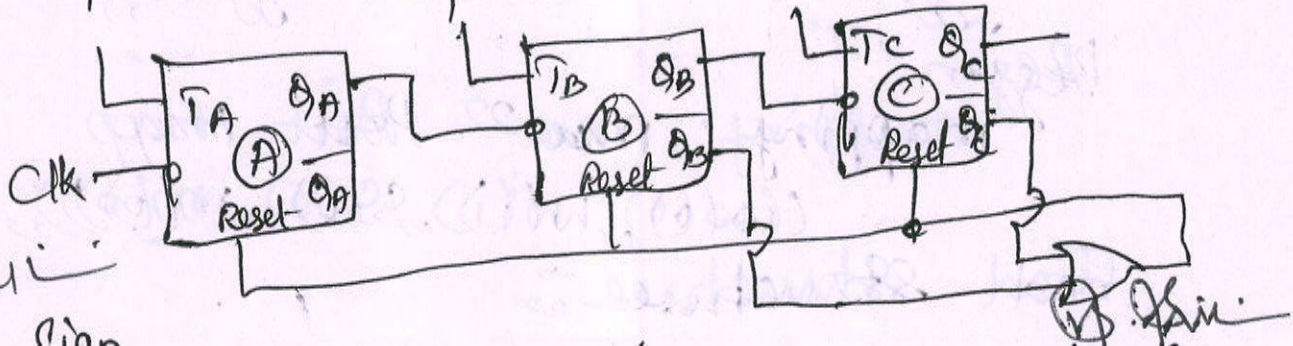
(3) b) ii)

Q_C	Q_B	Q_A	Reset logic
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

K-map



$Y = \overline{Q_C} + \overline{Q_B}$



R. Rupini
Staff Sign

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Cycle Test Answer Book

Name	NISHA K			**Year/ Semester**	II / IV
Reg No.	912618105005	**Date/Session**	12.10.19 / FN	**Department**	EEE
Course code	EE8351	**Course Title**	Digital Logic circuits		
Cycle Test		**CT 1** ☐	**CT 2** ☐	**CT 3** ☑	**Model** ☐
Name and Signature of the Invigilator with date		Shri 12/10/19 [RAMESH RAJA.S]			

Instruction to the Student: Put tick mark to the question attended in the column against question.

Part A			Part B / Part C					Total Marks
Q. No.	✓	Marks	Q. NO.	✓	a Marks	✓	b Marks	
1	✓	2	11	✓	12			12
2	✓	2	12			✓	12	12
3	✓	2	13	✓	12			12
4	✓	2	14					
5	✓	2	15					
6	✓	2	16					
7	✓	2					Grand Total	36
8	✓	2						
9	✓	2						
10	✓	2						
Total		20						

94%

Grand Total

(MRS. R. RAGADHARSHINI)
R. R
18/10/19

Name and Signature of the Examiner with date

To be filled by the examiner

Course Outcomes	1	2	3	4	5	6	Total
Marks allotted				23	37		60
Marks Obtained				22	34		56

IQAC Audit - Remarks

P. SUBHA

28/10/19

Name and Signature of the IQAC member

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KAIKKURICHI, PUDUKKOTTAI – 622 303

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
ACADEMIC YEAR 2019 – 2020 (ODD SEMESTER)
STUDENTS MARK STATEMENT- CO BASED
CYCLE TEST-III

SUBJECT CODE &TITLE: EE8351 & Digital Logic Circuits

YEAR/SEM: II/III **MONTH & YEAR: OCT & 2019**

S.NO	REG NO	STUDENT NAME	C202.4 (23)	C202.5 (37)	TOTAL (60)	TOTAL (100)
1.	912618105001	AARTHI G	22	32	54	91
2.	912618105002	AASHA R	20	37	57	95
3.	912618105003	AGARI S	21	35	56	94
4.	912618105004	JEEVITHA R	22	35	57	95
5.	912618105005	NISHA K	22	34	56	94
6.	912618105006	RAMANA R	20	35	55	92
7.	912618105007	SNEHA S	20	33	53	90
8.	912618105301	VINOTHINI V	10	16	26	43

MARKS RANGE:

<20	20-30	31-40	41-50	51-60	61-70	71-80	81-90	91-100
–	–	–	1	–	–	–	1	6

Total No.of Candidates Present	08
Total No.of Candidates Absent	NIL
Total No.of Students Pass	07
Total No. of Students Fail	01
Percentage of Pass	87.5%

Faculty Incharge

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PUDUKKOTTAI DISTRICT

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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ROOT CAUSE ANALYSIS

Name of the Faculty : Mrs. R. RAGHADHARSHINI Course Code & Name: EE8351 & Digital Logic Circuits

Degree & Program : B.E & EEE Semester : III

Cycle Test : I /II/III Exam/Month & Year : OCT & 2019

Target : 100 % Achieved : 87.5 %

S.NO	REG NO	NAME OF THE STUDENT	CAUSES FOR FAILURE	CORRECTIVE ACTION TAKEN
1.	912618105301	VINOTHINI V	Due to health issue	Advised to take care of health and study well.
2.				
3.				
4.				
5.				
6.				

R. Raghadharshini

Signature of the Faculty Member

Signature of the HoD/EEE

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Circular Date: 19.10.2019

Retest for third cycle test will be conducted from 21.10.2019 to 23.10.2019 for the III, V & VII semester (II, III & IV year) students.

The following instructions are to be followed by the faculty members.

- Total marks for which the question paper to be set will be for 50 marks. **(PART A** 5X2=10, **PART B** 2X13=26 **& PART C** 1X14=14**)**
- It is the responsibility of the **question paper** setter to take the Xerox copies of the required number of question papers.
- Concerned Faculty members are requested to conduct the examination as per the scheduled and handover the valued answer scripts to the students on or before 24.10.2019.

PRINCIPAL

19/10/19

Cc:

- All faculty
- Exam cell
- Office file

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Kaikkurichi - 622 303, Pudukkottai Dt.

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN
KAIKKURICHI, PUDUKKOTTAI – 622 303.

Circular

Date: 19.10.2019

Retest for third cycle test will be conducted from 21.10.2019 to 23.10.2019 for the III semester (II year) B.E students for 50 marks as per the time table given below. Students are directed to prepare well and score good marks.

Date	10.00 am -11.30 am	2.30 pm -04.00 pm
21.10.2019	MA8353-Transforms and Partial Differential Equations (CIVIL/EEE) EC8393-Fundamentals of Data Structures in C (ECE) EC8395-Communication Engineering(CSE)	CE8391-Construction Materials (CIVIL) EC8351-Electronic Circuits I (ECE) ME8792-Power Plant Engineering (EEE)
22.10.2019	CE8301-Steength of Materials-I (CIVIL) CS8351-Digital Principles and System Design (CSE) EC8352- Signals and Systems (ECE) EC8353-Electron Devices and Circuits(EEE)	CE8351-Surveying(CIVIL) CS8391-Data Structures-(CSE) EC8391-Control System Engineering (ECE) EE8301-Electrical Machines-I(EEE)
23.10.2019	CE8302-Fluids Mechanics(CIVIL) MA8351-Discrete Mathematics (CSE) MA8352- Linear Algebra and Partial Differential Equations (ECE) EE8351-Digital Logic Circuits(EEE)	CE8392-Engineering Geology (CIVIL) CS8392-Object Oriented Programming(CSE) EC8392-Digital Electronics (ECE) EE8391-Electromagnetic Theory(EEE)

PRINCIPAL

15/10/19

Cc:

- All II year B.E Classes
- All faculty
- Exam cell
- Notice Board
- Office file

Dr. S.THILAGAVATHI M.E.,Ph.D.,
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Register Number:												

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Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Cycle Test – III (Retest)			Date/Session	23.10.2019/FN	Marks	50
Course code	EE8351	Course Title	DIGITAL LOGIC CIRCUITS			
Regulation	2017	Duration	90 minutes	Academic Year	2019-2020	
Year	II	Semester	III	Department	EEE	

COURSE OUTCOMES

CO1:	Comprehend various number systems and simplify the logical expressions using Boolean functions.
CO2:	Explain about the combinational circuits.
CO3:	Design various synchronous sequential circuits.
CO4:	Develop the asynchronous sequential circuits.
CO5:	Describe about PLDs and FPGA.
CO6:	Demonstrate the digital simulation for development of application oriented logic circuits.

Q.No.	Question	CO	BTS
	PART A (Answer all the Questions 5 x 2 = 10 Marks)		
1	What is state equivalence theorem?	C202.4	K1
2	What is pulse mode circuit?	C202.4	K1
3	What is Switch-level modeling?	C202.4	K1
4	List the different techniques used for state assignment.	C202.5	K1
5	What are identifiers?	C202.5	K1
	PART B (Answer all the Questions 2 x 13 = 26 Marks)		
6a	Describe the steps involved in design of asynchronous sequential circuit in detail with an example.	C202.4	K2
	OR		
6b	i) Write program in HDL to design 2 bit up/down counter. ii) Write the HDL program for 2:1 multiplexer in Dataflow and Behavioural description.	C202.4	K2
7a	Write the VHDL program for 4 bit counter.	C202.5	K2
	OR		
7b	Explain the various modeling methods used in VHDL with an example.	C202.5	K2
	PART C (Answer all the Questions 1 x 14 = 14 Marks)		
8a	i)Draw the VLSI design flowchart used for IC design and fabrication. ii) Write down a VHDL code for 8:1 multiplexer.	C202.5	K2
	OR		
8b	i)Differentiate PAL and PLA implementations with the help of the same example $F_2(a,b,c) = \Sigma(0,1,3,4,6,7)$. ii) Design a Modulo-6 asynchronous binary up-counter	C202.5	K2

R.R 22/10/19

Course Faculty

(Name /Sign / Date)

(Mrs. R. RAGHADHARSHINI)

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22/10/19

HoD

(Name /Sign / Date)

(Mrs. S. SUSILADEVI)
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KAIKURICHI, PUDUKKOTTAI -622 303

ACADEMIC YEAR 2019-2020--- ODD SEMESTER

ATTENDANCE SHEET FOR RETEST

RETEST FOR CYCLE TEST-III

PROGRAM : B.E / EEE
YEAR/SEM : II/III
SUBJECT CODE & TITLE : EE8351 & Digital Logic Circuits
DATE : 23/10/19

SI .NO	REG.NO	NAME	SIGNATURE
1	912618105301	VINOTHINI V	V. Vinothini

R. Ramalakshmi

SIGNATURE OF THE FACULTY

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Cycle Test (Retest) Answer Book

Name	VINOTHINI V			**Year/ Semester**	II / III
Reg. No	912618105301	**Date/Session**	28/10/19/FN	**Department**	EEE
Course code	EE8351	**Course Title**	Digital Logic Circuits		
Cycle Test (Retest)	**CT 1** ☐	**CT 2** ☐	**CT 3** ☑	**Model** ☐	
Name and Signature of the Invigilator with date	R. Ragadharshini (Mrs. R. Ragadharshini) 23/10/2019				

Instruction to the Student: Put tick mark to the question attended in the column against question.

Part A			Part B / Part C					Total Marks
Q. No.	✓	Marks	Q. NO.	✓	a Marks	✓	b Marks	
1	✓	2	11	✓	12			12
2	✓	2	12	✓	11			11
3	✓	2	13			✓	12	12
4	✓	2	14					
5	✓	2	15					
6			16					
7			Grand Total					35
8								
9								
10								
Total		10	90% Grand Total				R. Ragadharshini 24/10/19 (Mrs. R. Ragadharshini) Name and Signature of the Examiner with date	

To be filled by the examiner

Course Outcomes	CO1	CO2	CO3	CO4	CO5	CO6	Total
Marks allotted				19	31		50
Marks Obtained				18	27		45

IQAC Audit - Remarks

P. SUBHA 28/10/19
Name and Signature of the IQAC member

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KAIKKURICHI, PUDUKKOTTAI – 622 303
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
ACADEMIC YEAR 2019 – 2020 (ODD SEMESTER)

STUDENTS MARK STATEMENT- CO BASED

CYCLE TEST-III (Retest)

SUBJECT CODE &TITLE: EE8351 & Digital Logic Circuits

YEAR/SEM: II/III **MONTH & YEAR: OCT & 2019**

S.NO	REG NO	STUDENT NAME	C202.4 (19)	C202.5 (31)	TOTAL (50)	TOTAL (100)
1.	912618105301	VINOTHINI V	18	27	45	90

MARKS RANGE:

<20	20-30	31-40	41-50	51-60	61-70	71-80	81-90	91-100
–	–	–	–	–	–	–	1	–

Total No.of Candidates Present	1
Total No.of Candidates Absent	NIL
Total No.of Students Pass	1
Total No. of Students Fail	NIL
Percentage of Pass	100%

R. R

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PUDUKKOTTAI DISTRICT

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ACADEMIC YEAR 2019 – 2020 (ODD SEMESTER)

FINAL INTERNAL STUDENTS MARK STATEMENT(Out of 20)

SUBJECT CODE &TITLE: EE8351 & Digital Logic Circuits

YEAR/SEM: II/III

S.NO	REG NO	STUDENT NAME	TOTAL (20)
1.	912618105001	AARTHI G	17
2.	912618105002	AASHA R	18
3.	912618105003	AGARI S	18
4.	912618105004	JEEVITHA R	19
5.	912618105005	NISHA K	18
6.	912618105006	RAMANA R	18
7.	912618105007	SNEHA S	17
8.	912618105301	VINOTHINI V	17

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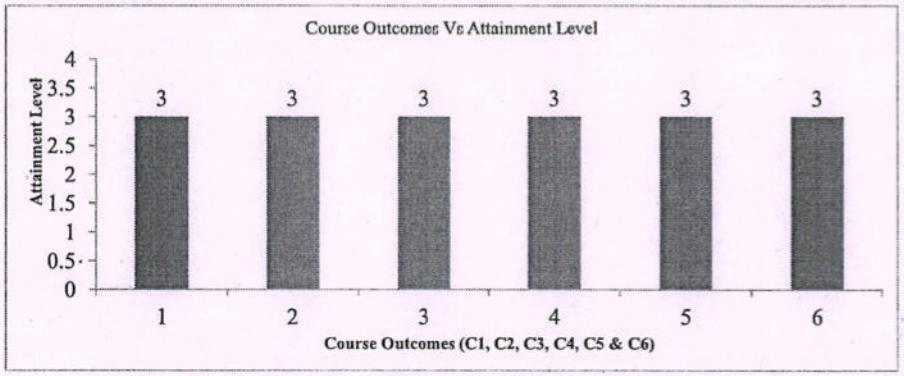
Department of Electrical and Electronics Engineering

Internal Assessment -Attainment of Course Outcomes (Through Direct Assessment)

ACADEMIC YEAR - 2019 - 2020		BATCH	2018 - 2022					
COURSE CODE/TITLE	EE8351 / DIGITAL LOGIC CIRCUITS	COURSE OUTCOME	1	2	3	4	5	6
YEAR/SEM	II/III	TARGET(%)	65	65	65	65	65	65
COURSE COORDINATOR	RAGADHARSHINI.R	TOTAL STRENGTH	8					

ATTAINMENT LEVEL	Level	Range
	1	UP TO 60% of the students scored more than target
	2	61 - 79% of the students scored more than target
	3	80% & ABOVE of the students scored more than target

S.NO	REG NO	NAME OF THE STUDENT	IAT 1 - MARKS ALLOTED						IAT 2 - MARKS ALLOTED						IAT 3 - MARKS ALLOTED						Assignment / Mini Project /Tutorial / Seminar						TOTAL COURSE OUTCOME					
			C1	C2	C3	C4	C5	C6	C1	C2	C3	C4	C5	C6	C1	C2	C3	C4	C5	C6	C1	C2	C3	C4	C5	C6	C1	C2	C3	C4	C5	C6
			60	40							40	60							60	40		10	10			10	60	50	50	60	60	50
1	912618105001	AARTHI G	51	34							34	51							55	36		7	8			8	51	41	42	51	55	44
2	912618105002	AASHA R	52	35							36	53							57	38		9	8			7	52	44	44	53	57	45
3	912618105003	AGARI S	51	34							34	52							56	38		8	8			8	51	42	42	52	56	46
4	912618105004	JEEVITHA R	55	37							37	56							57	38		9	7			8	55	46	44	56	57	46
5	912618105005	NISHA K	53	36							37	55							56	38		9	9			9	53	45	46	55	56	47
6	912618105006	RAMANA R	51	34							36	54							55	37		9	8			9	51	43	44	54	55	46
7	912618105007	SNEHA S	48	32							34	51							54	36		9	7			9	48	41	41	51	54	45
8	912618105301	VINOTHINI V	48	32							33	50							54	36		8	9			9	48	40	42	50	54	45
CO's Target Value																											39.0	32.5	32.5	39.0	39.0	32.5
No. of Students scored above CO's Target Value																											8	8	8	8	8	8
Percentage of Students scored above Target																											100.0	100.0	100.0	100.0	100.0	100.0
CO Attainment																											3	3	3	3	3	3
CO attainment Values to plot the Graph																											3	3	3	3	3	3



Faculty Incharge

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DEPARTMENT OF EEE

COURSE OUTCOME ATTAINMENT - UNIVERSITY EXAMINATION

ACADEMIC YEAR : 2019 - 2020 (ODD SEM)

YEAR/SEM : II/III Batch: 2018-2022

SUBJECT : EE8351 - DIGITAL LOGIC CIRCUITS

CO Attainment Level: 1 - (UPTO 60%) 2- (61%-79%) 3-(80% and Above)

TOTAL STRENGTH : 8

S.NO	Register No	NAME	Univ. Grade
1	912618105001	AARTHI G	B
2	912618105002	AASHA R	B
3	912618105003	AGARI S	B
4	912618105004	JEEVITHA R	B
5	912618105005	NISHA K	B+
6	912618105006	RAMANA R	B
7	912618105007	SNEHA S	U
8	912618105301	VINOTHINI V	U

No. of O Grade	0	0
No. of A+ Grade	0	0
No. of A Grade	0	0
No. of B+ Grade	1	1
No. of B Grade	5	5
No. of U Grade	2	2
No. of UA Grade	0	0
Target for course outcome Attainment	60	8
No of students above the target	6	
CO-Attainment University (%)	75.00	

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Overall Attainment Sheet – COs - POs & PSOs attainment calculation

CO	CO-Attainment Internal (CO-INT) (Avg. Attainment of All section) (%)	CO-Attainment University (CO-UNI) (Avg. Attainment of All section) (%)	Direct CO Attainment (0.20xCO-INT + 0.80xCO-UNI) (%)	CO Attainment Level
C202.1	100.0	75.00	80.0	3
C202.2	100.0	75.00	80.0	3
C202.3	100.0	75.00	80.0	3
C202.4	100.0	75.00	80.0	3
C202.5	100.0	75.00	80.0	3
C202.6	100.0	75.00	80.0	3

Expected CO-PO Level

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C202.1	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.2	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.3	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.4	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.5	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.6	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202	**2**	**2**	**1**	**1**	**1**	**-**	**-**	**-**	**-**	**1**	**-**	**1**	**2**	**-**	**1**

PO Attainment Level

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C202.1	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.2	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.3	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.4	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.5	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202.6	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
C202	2	2	1	1	1	-	-	-	-	1	-	1	**2**	-	1

Attainment of POs and PSOs:

Course Code	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C202	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1
Attainment	2	2	1	1	1	-	-	-	-	1	-	1	2	-	1

Comments by Program Coordinator	1. 2.
Remarks by HoD	

R. Ragadharshini

Name and Signature of the Faculty Member

[R. RAGADHARSHINI]

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